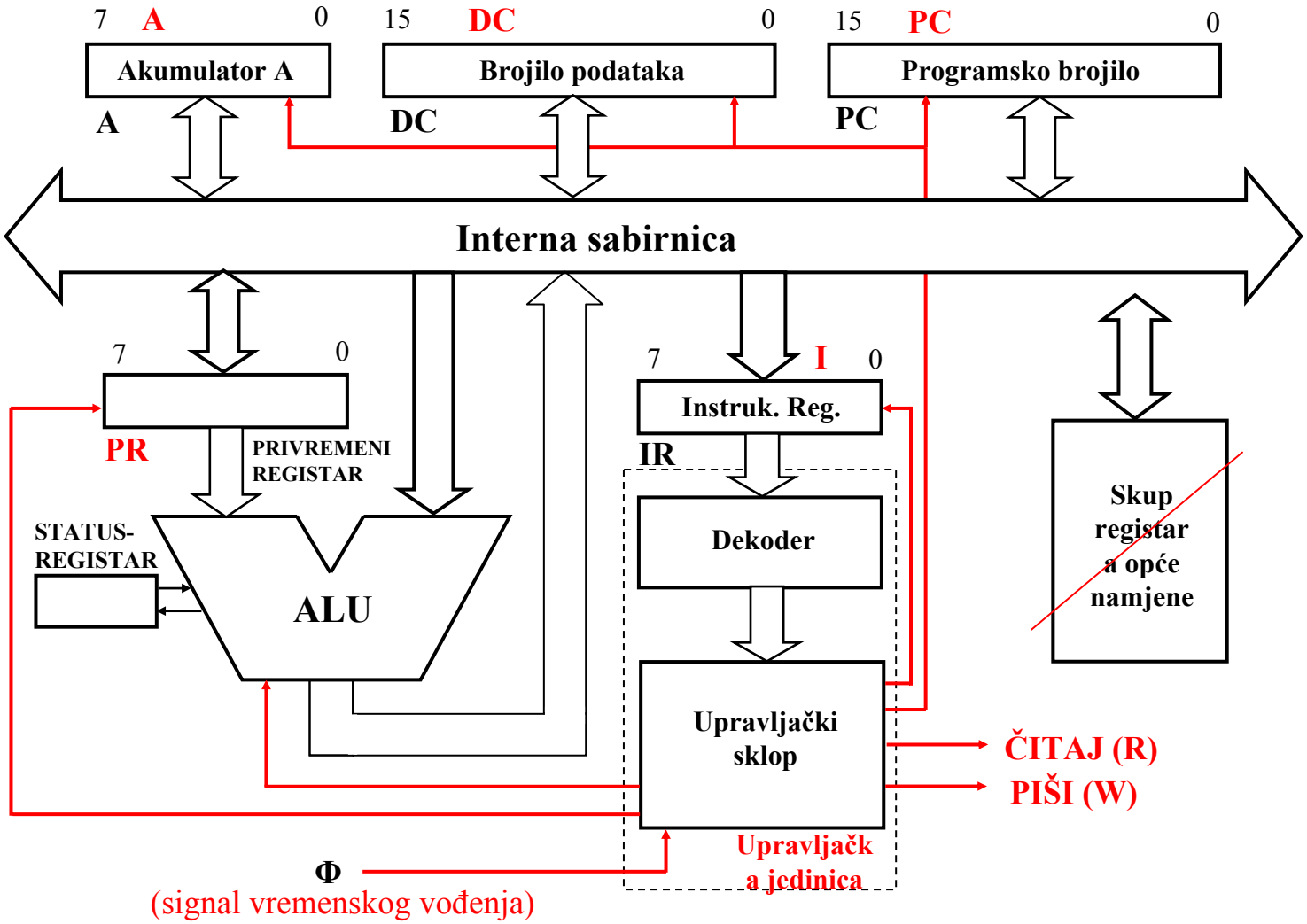
3. Pojednostavnjeni modeli CISC I RISC procesora

- Komponente modela CISC
- Primjer izvođenja programa
- Stanje registara
- Stanje na sabirnicama
- Komponente modela (S)RISC
- ISA-model procesora

Model (mikro)procesora CISC arhitekture

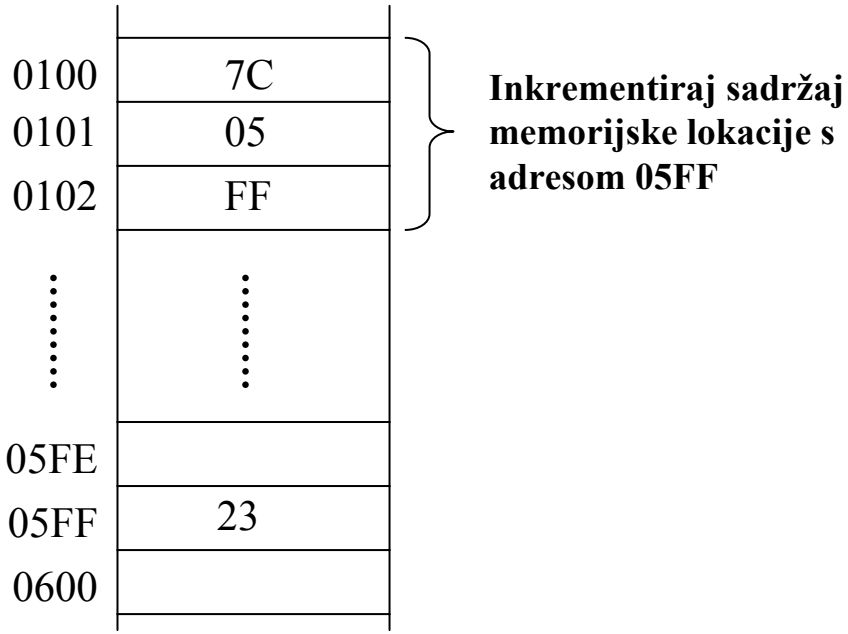


Komponente modela

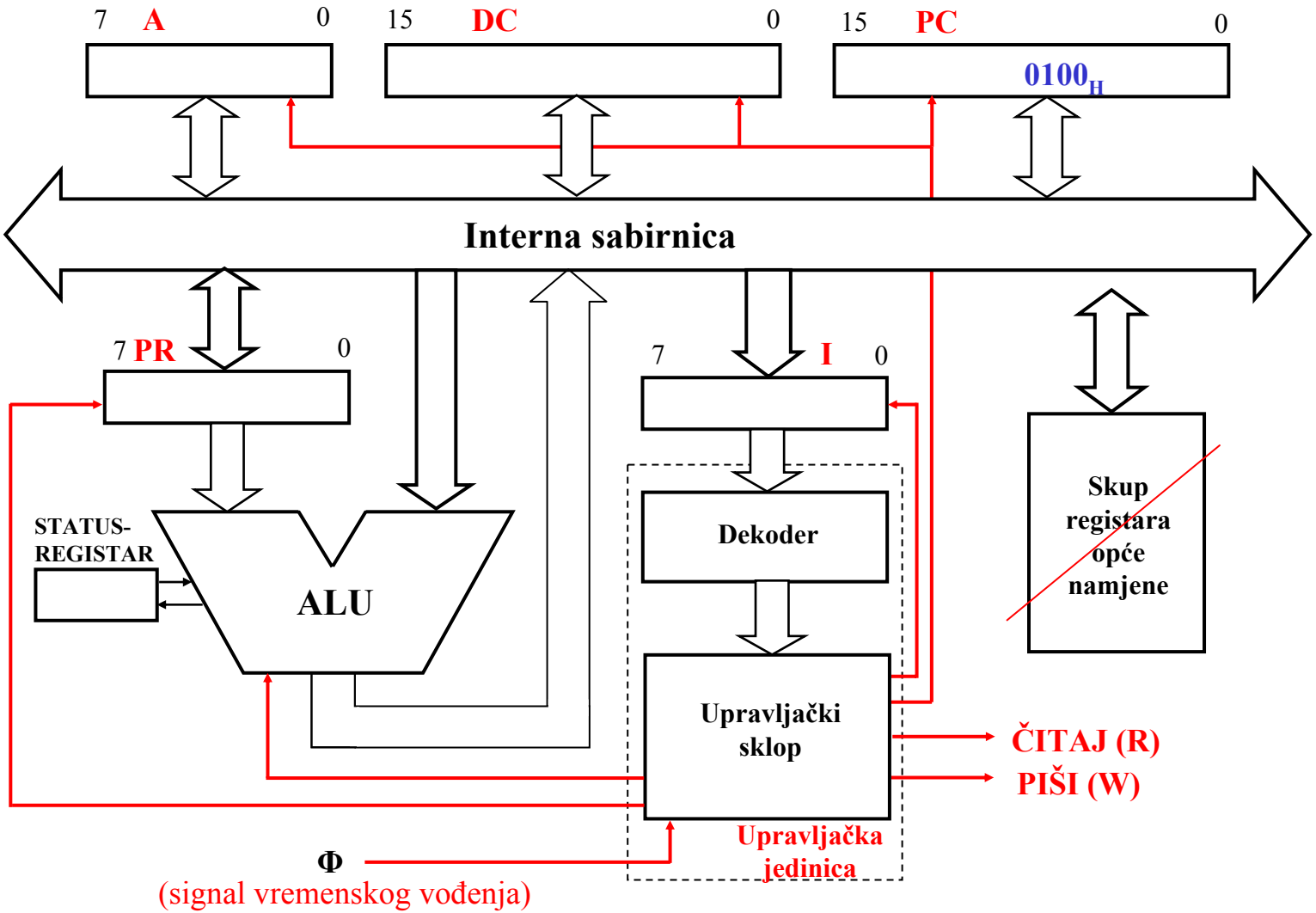
- Akumulator A
- Programsko brojilo PC
- Instrukcijski registar IR
- Brojilo podataka DC
- Privremeni registar PR
- Status-registar (Registar stanja)
- ALU
- (Skup registara opće namjene)
- Interna sabirnica
- Upravljačka jedinica

Primjer programa:

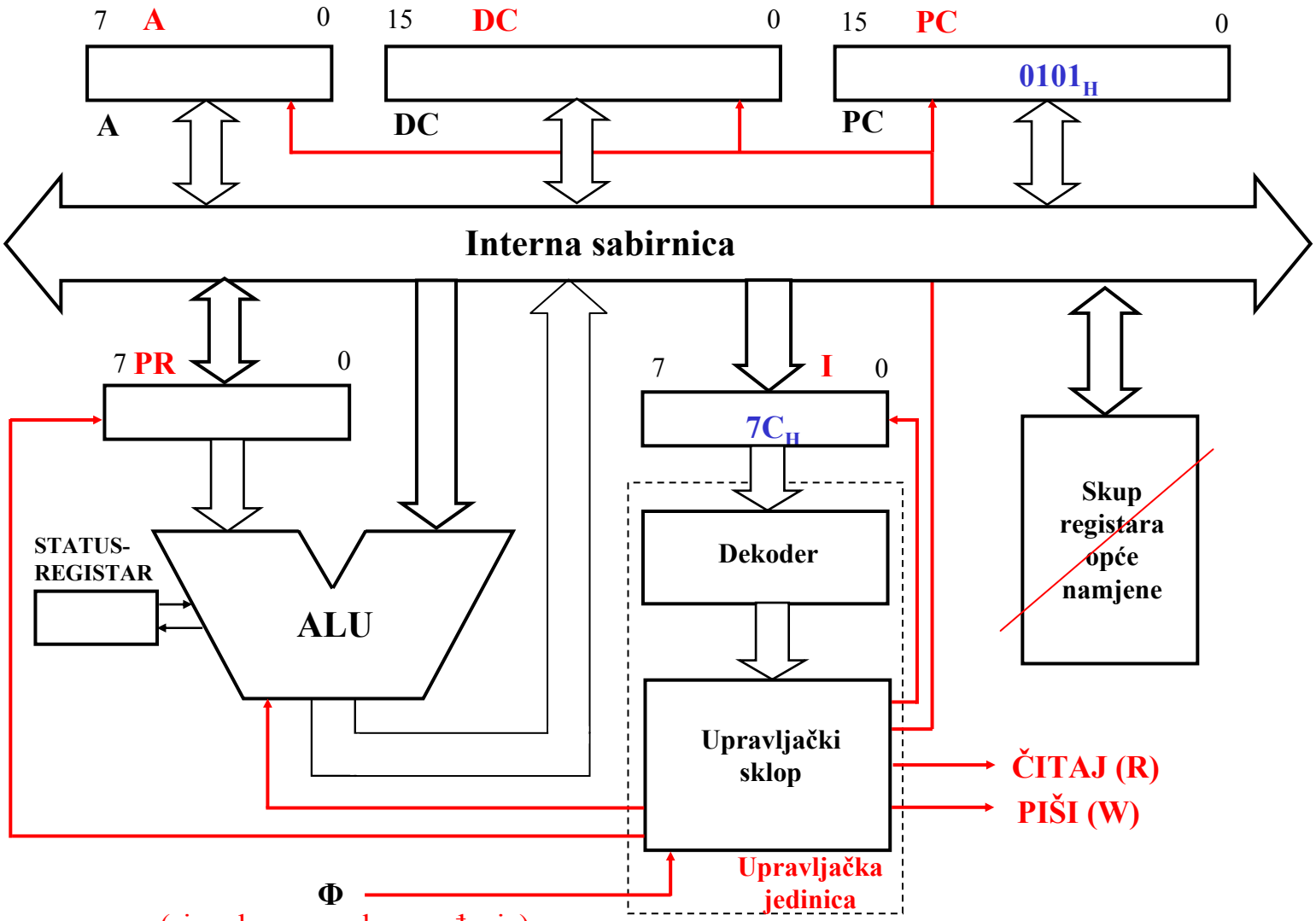
- Program samo od jedne instrukcije INC $05FF

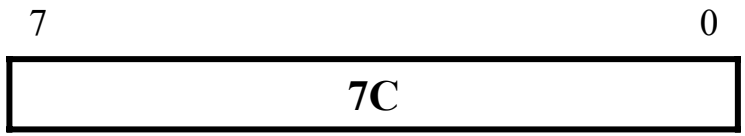


Početni uvjeti



Stanje nakon pribavljanja operacijskog koda instrukcije





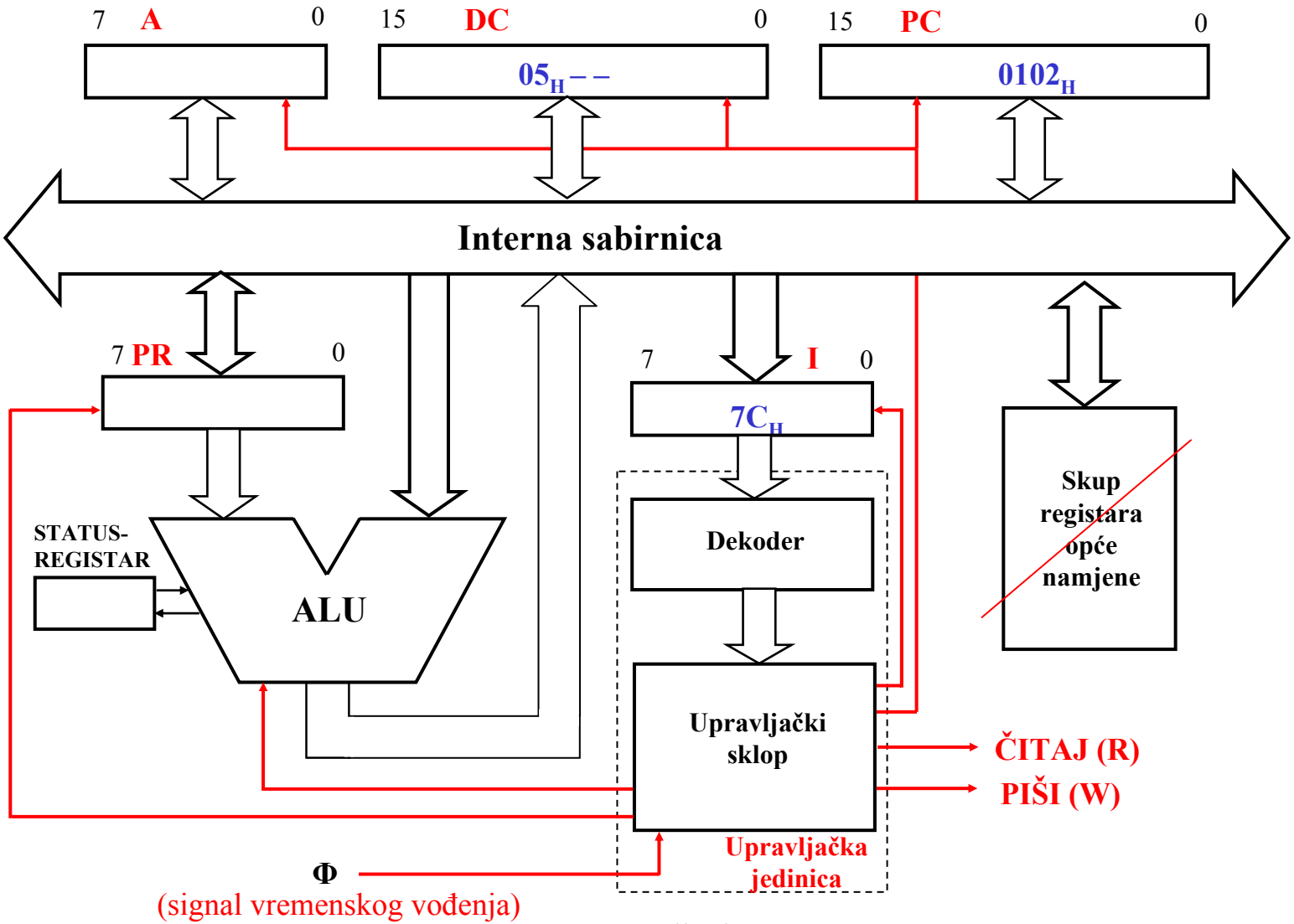
Operacijski kod

7C = 01111100

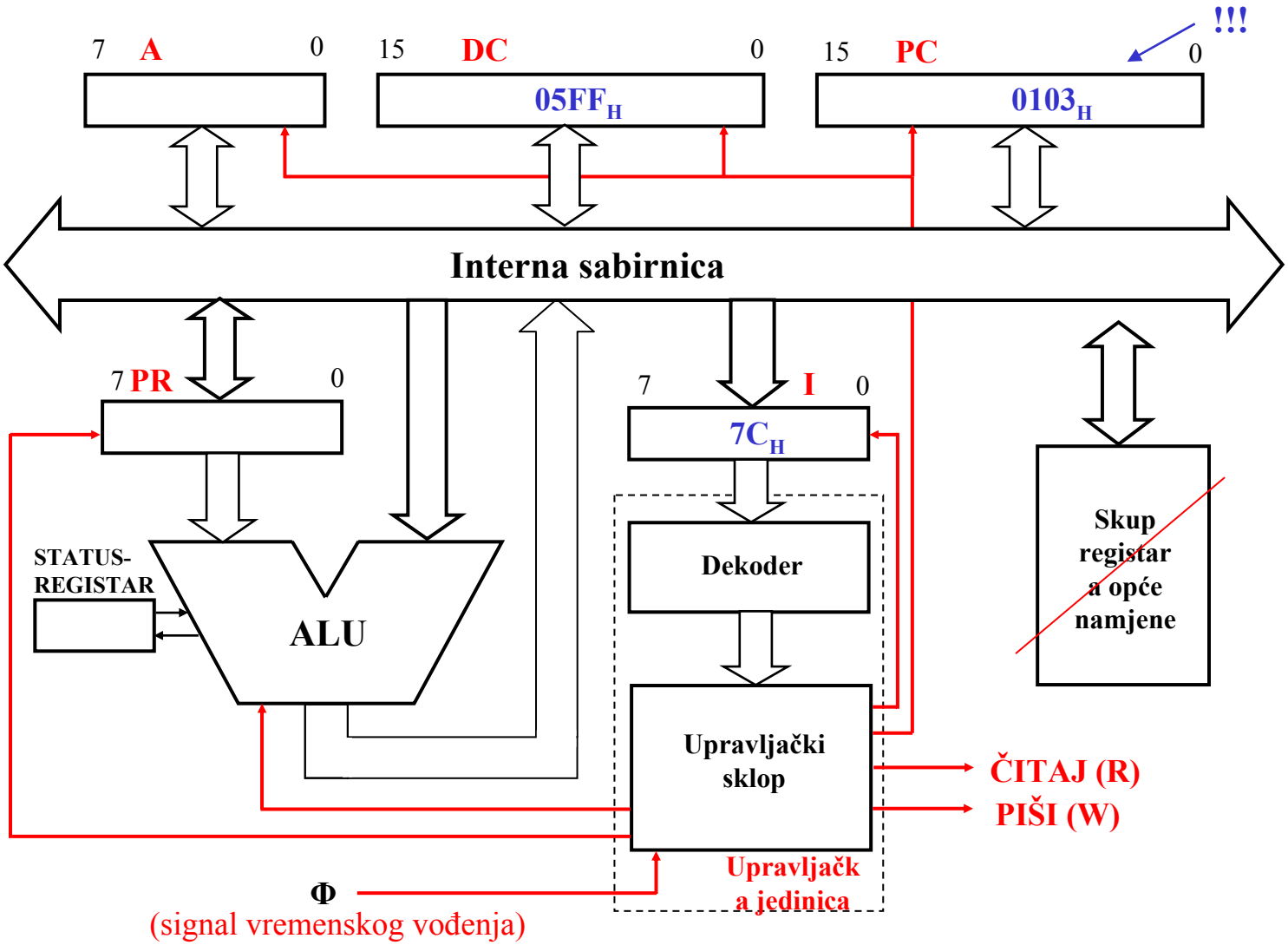
se tumači kao: Povećaj za 1 vrijednost operanda čija je adresa sadržana u dva bajta koja slijede ovom operacijskom kodu.

Stanje nakon pribavljanja značajnijeg bajta adrese operanda

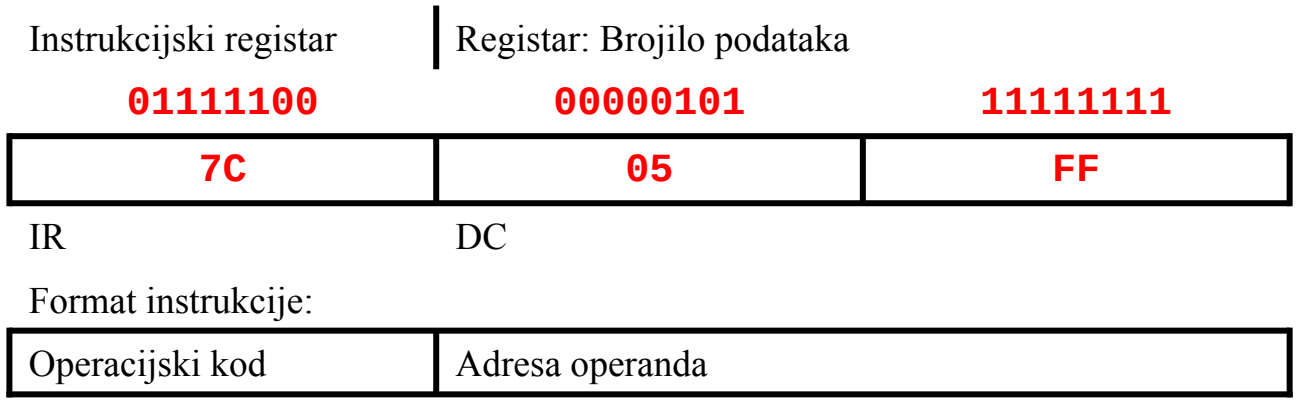
Pazi: Faza Pribavi još uvijek traje!



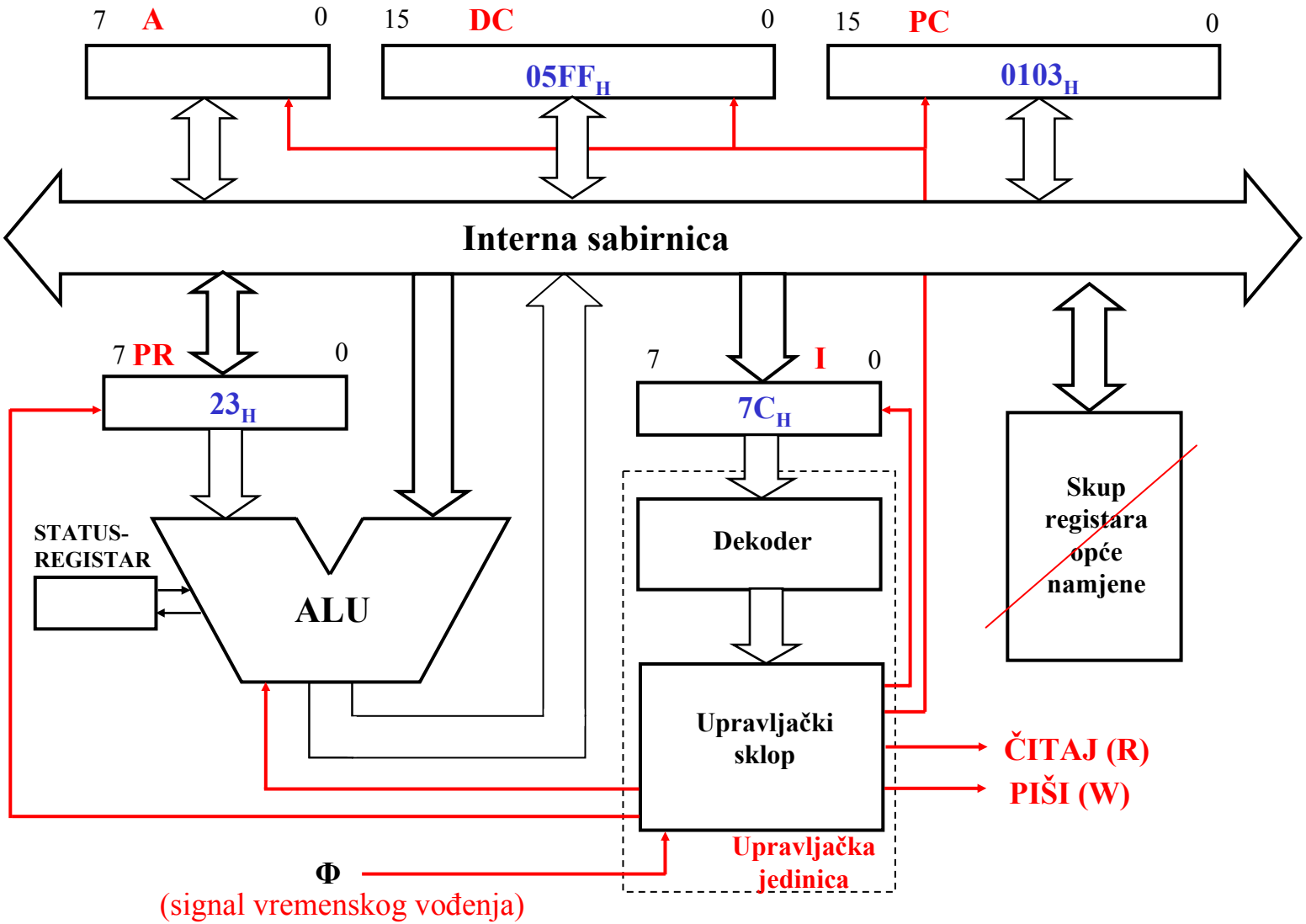
Stanje nakon pribavljanja manje značajnijeg bajta adrese operanda



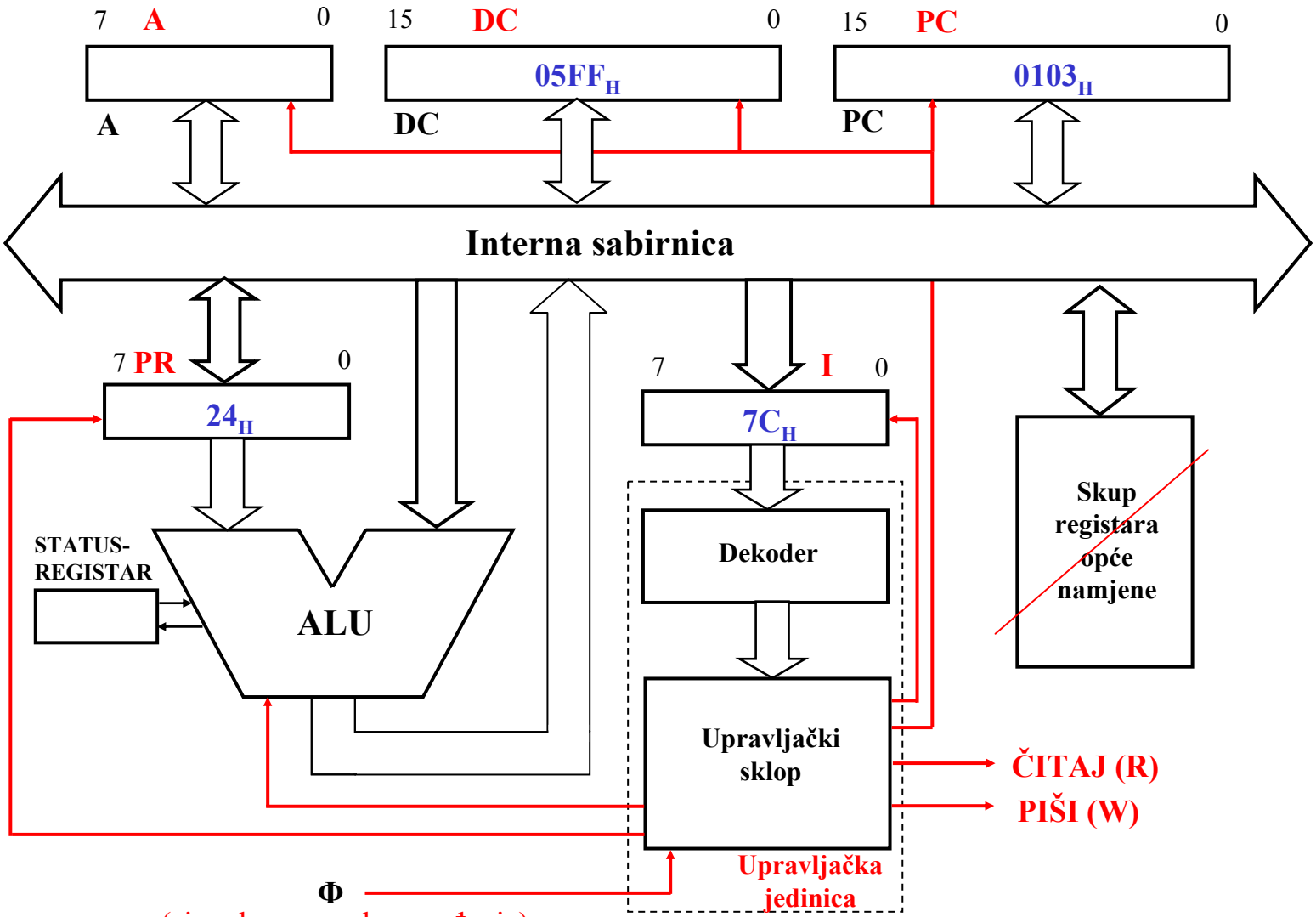
Faza Pribavi je završena!



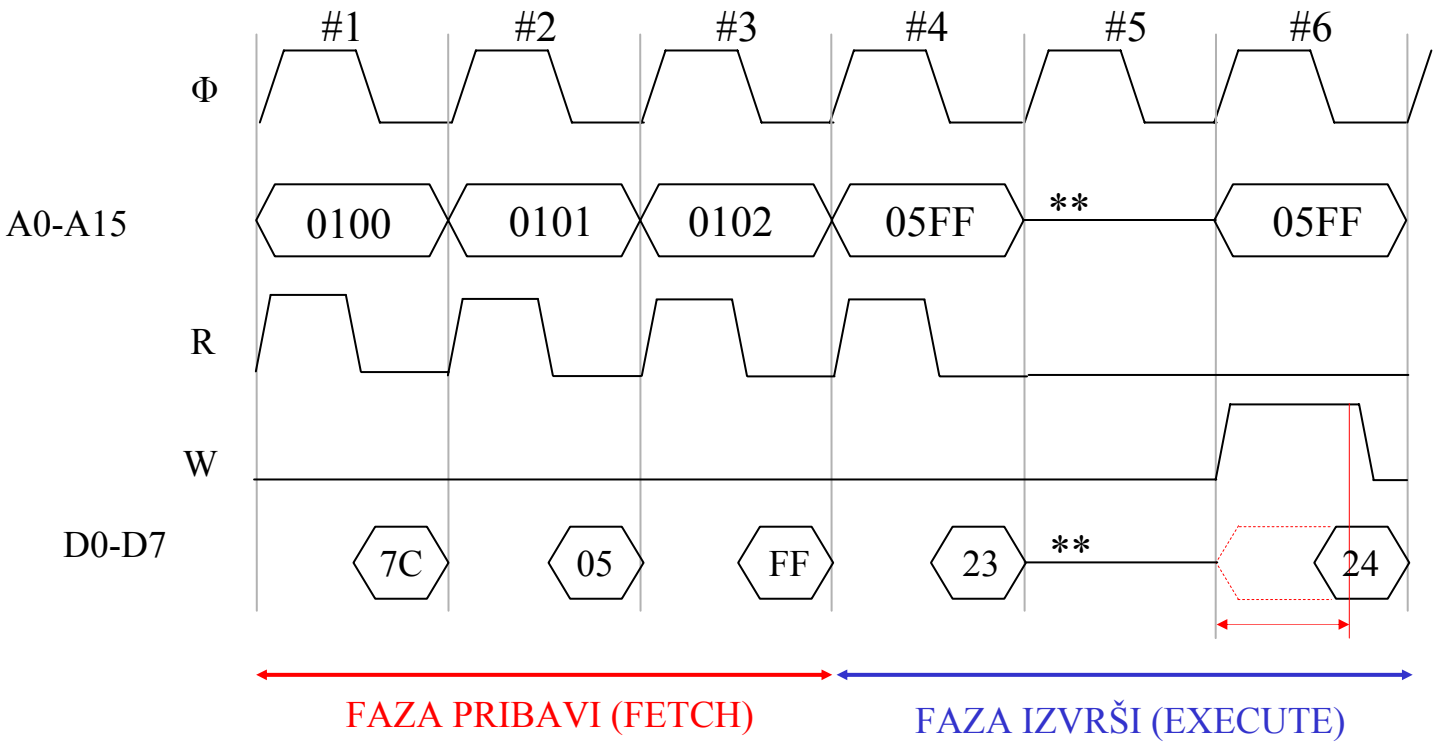
Stanje nakon dohvata operanda (faza IZVRŠI)



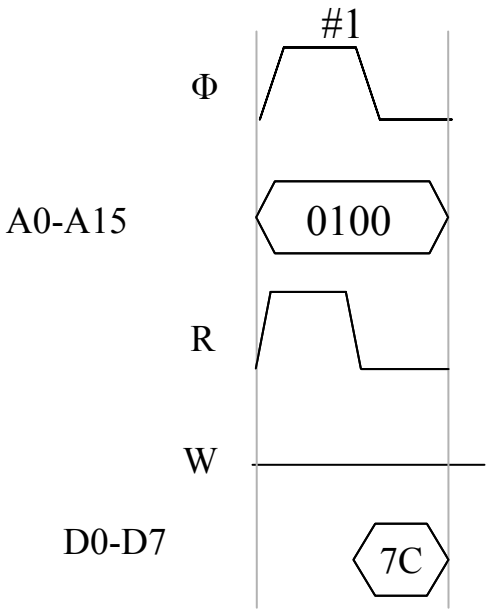
Stanje nakon povećanja operanda za jedan (faza IZVRŠI)



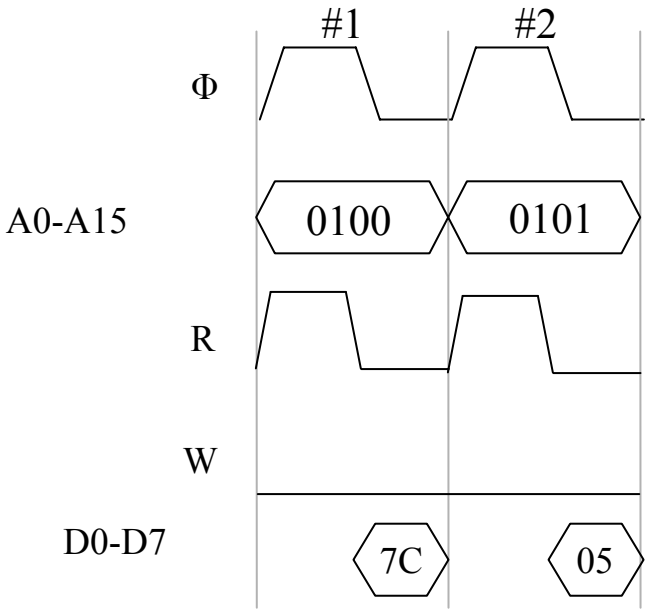
Stanje na vanjskim sabirnicama



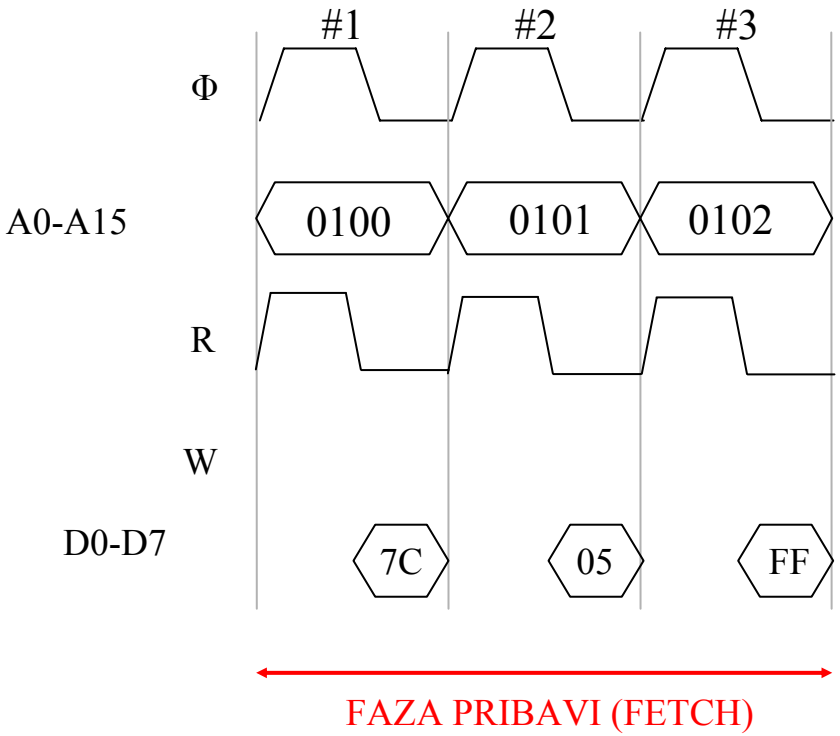
Prva perioda signala vremenskog vođenja



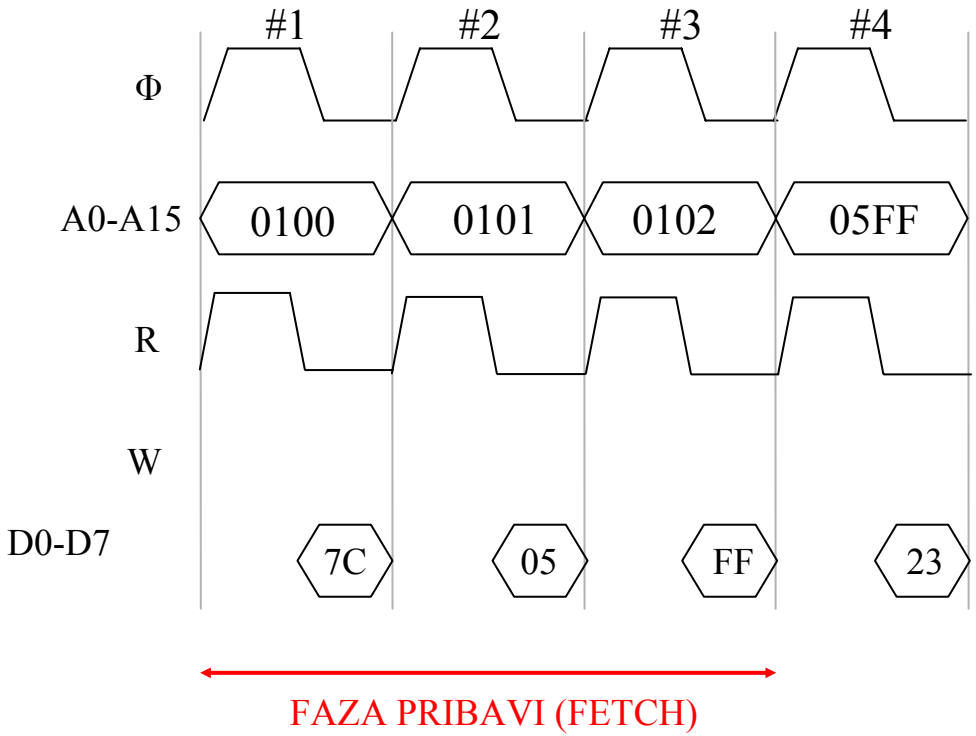
Druga perioda signala vremenskog vođenja



Treća perioda signala vremenskog vođenja



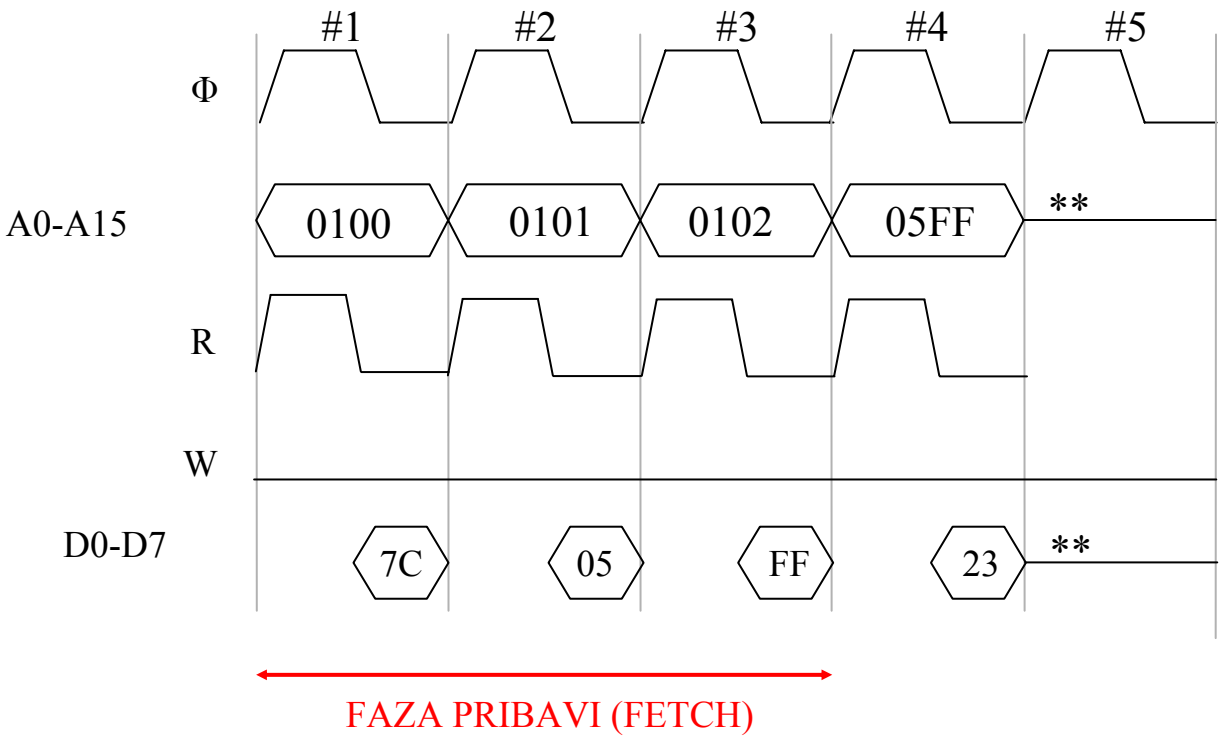
Četvrta perioda signala vremenskog vođenja



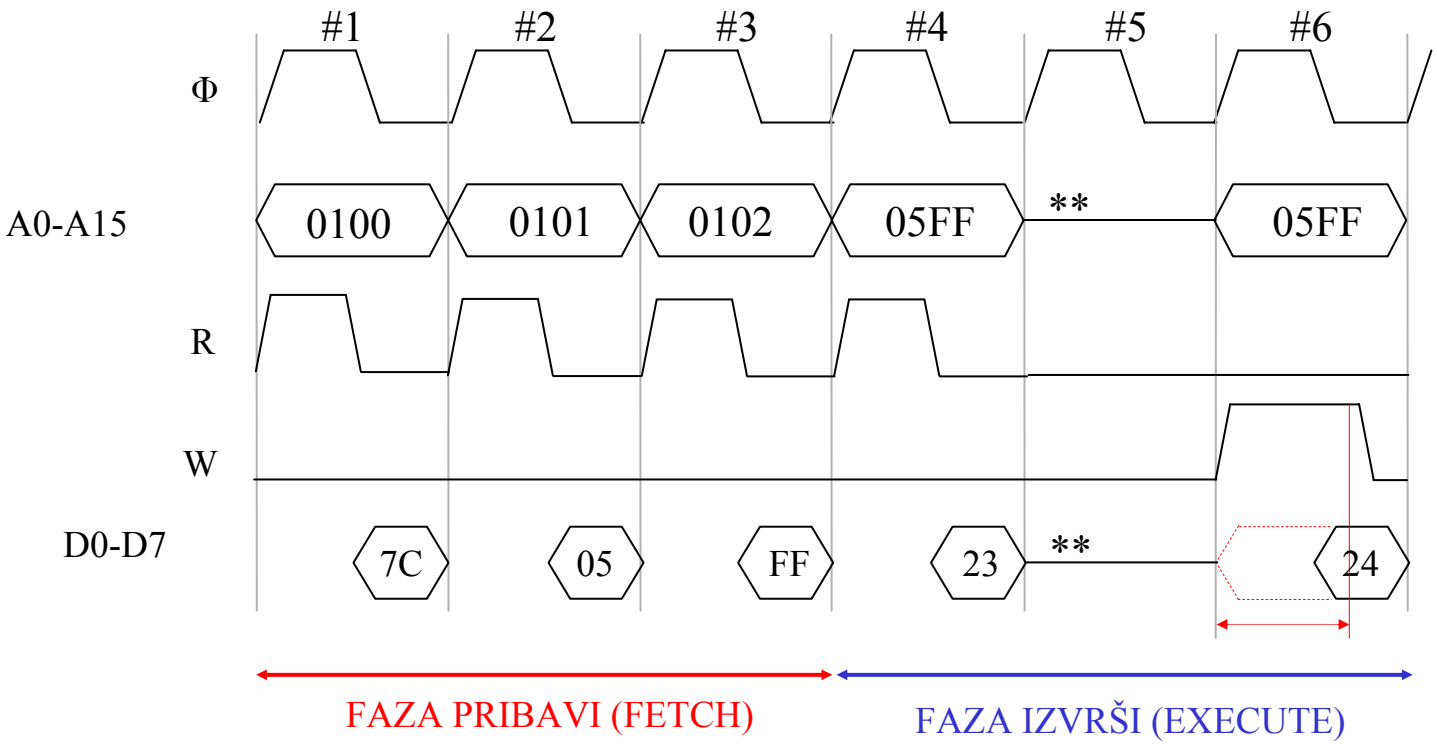
Peta perioda signala vremenskog vođenja

Pozor:

** - Označava stanje visoke impedancije /treće stanje/



Šesta perioda vremenskog vođenja



Motorola MC 6800

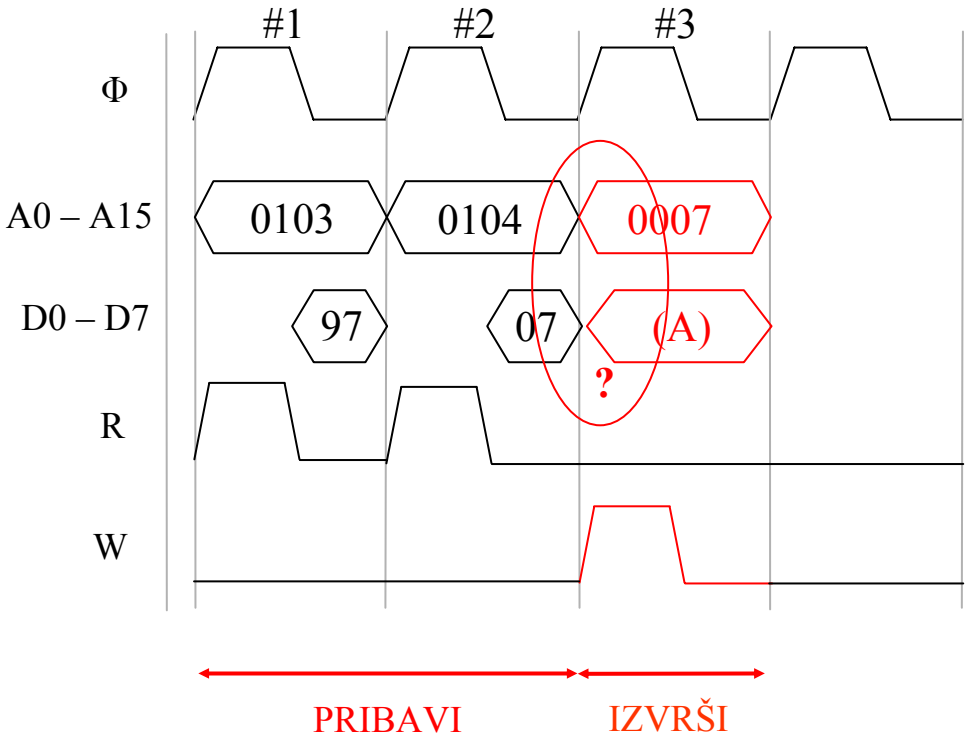
(izravni prošireni način adresiranja)

	OP	~	#
INC	7C	6	3

Zahtijeva 6 periode signala vremenskog vođenja!

Naš model obavlja ovu instrukciju također za 6 perioda!

Stanje na sabirnicama za instrukciju STA $07



Motorola MC 6800

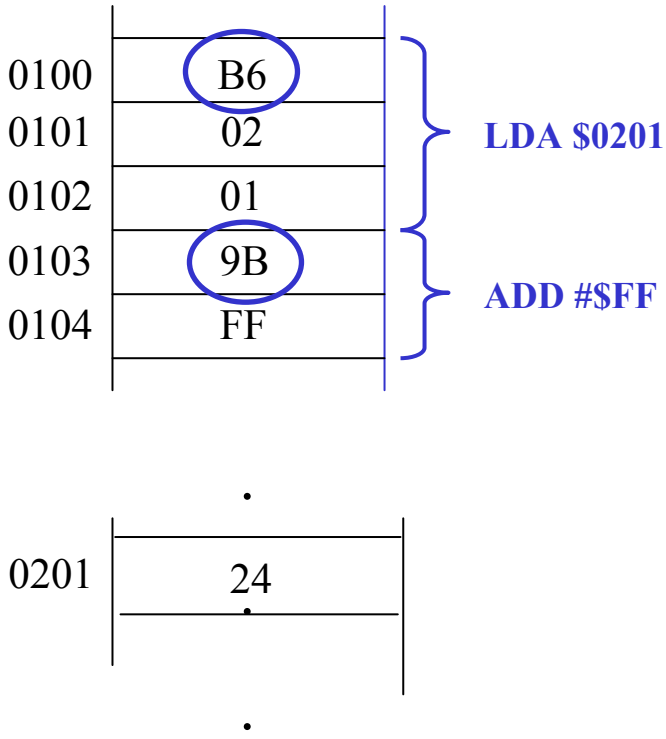
(izravni način adresiranja)

	OP	~	#
STA A	97	4	2

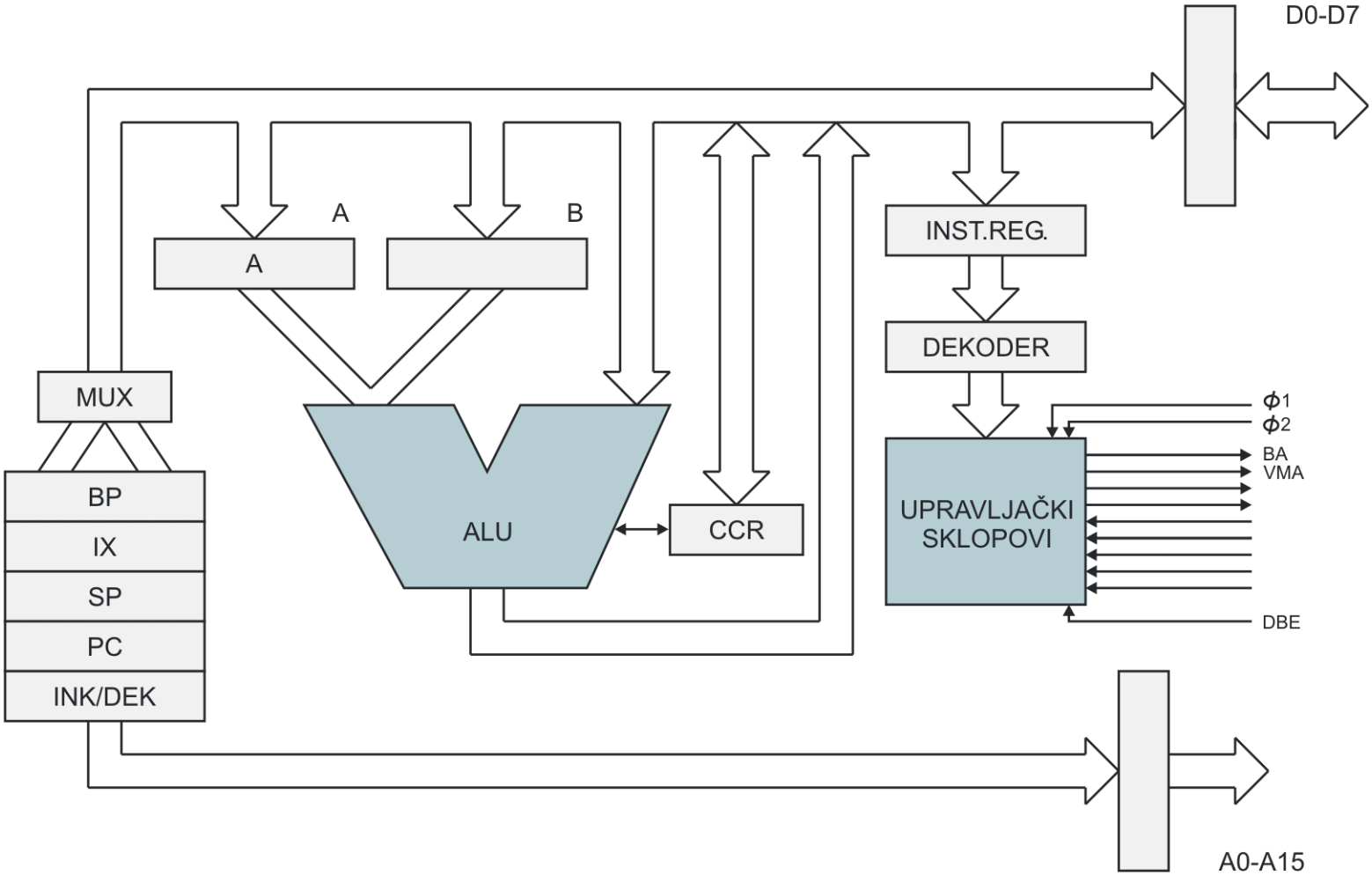
Zahtijeva 4 periode signala vremenskog vođenja!

Naš model obavlja ovu instrukciju tijekom 3 periode?!

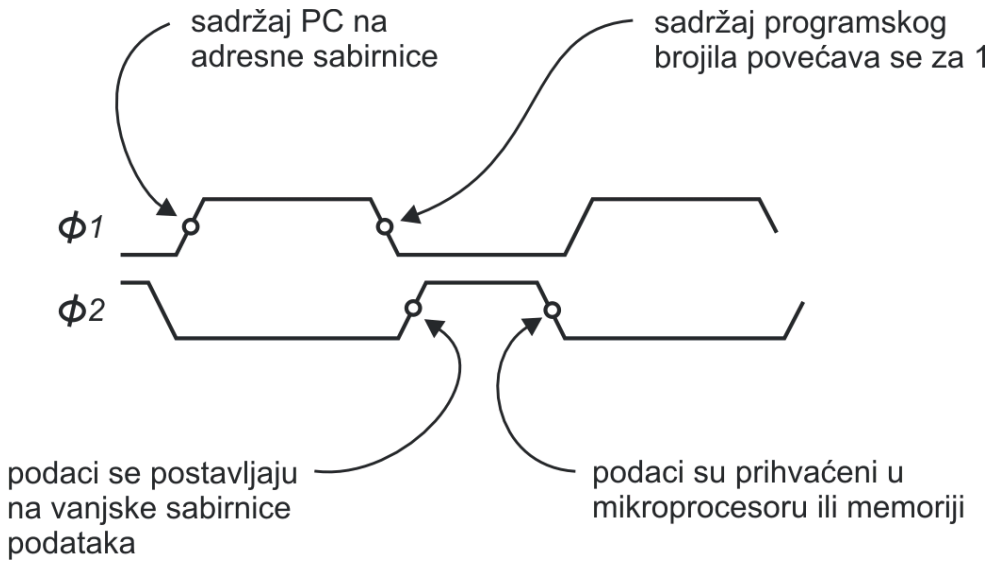
Primjer:



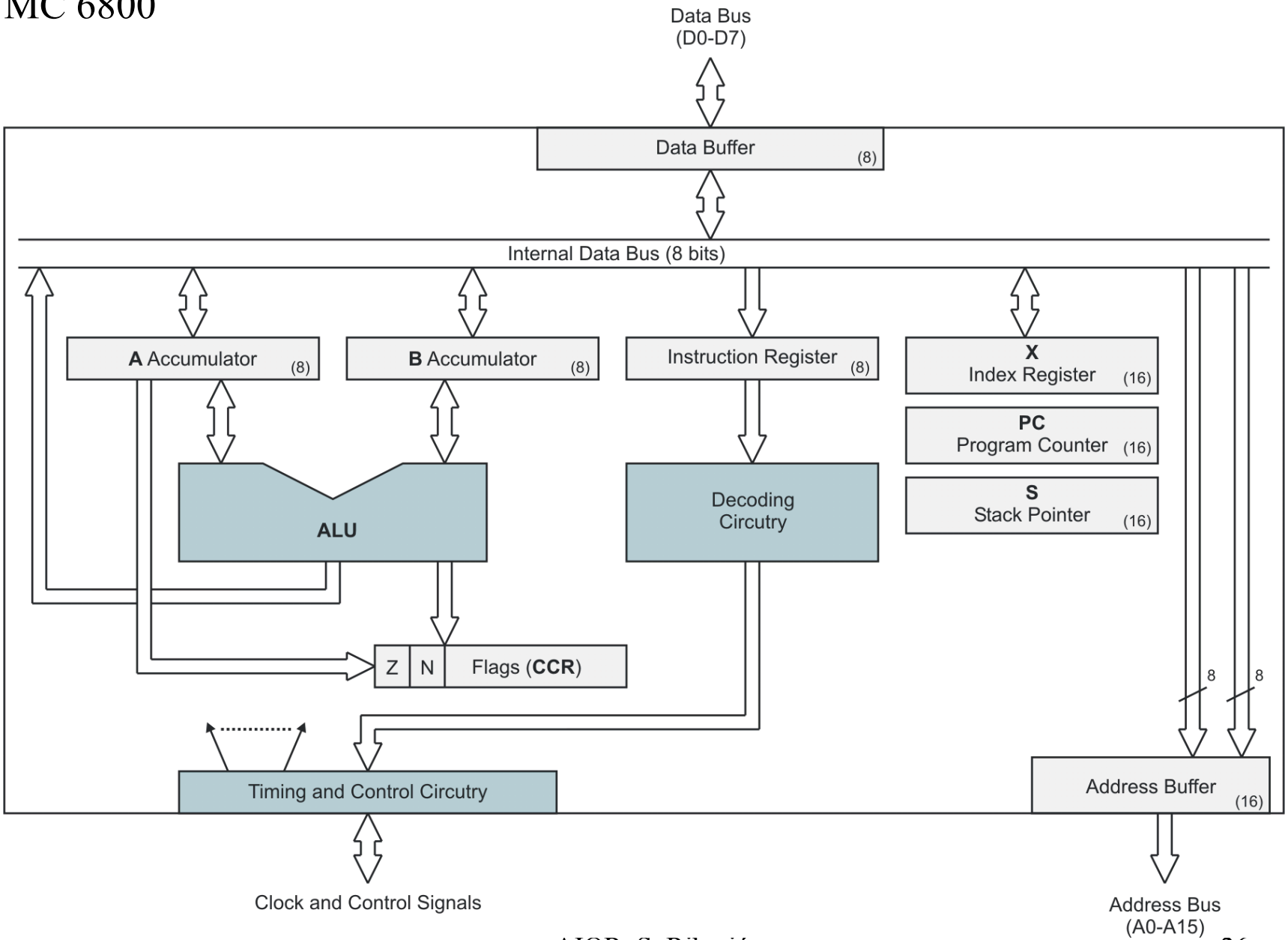
Primjer: MC 6800



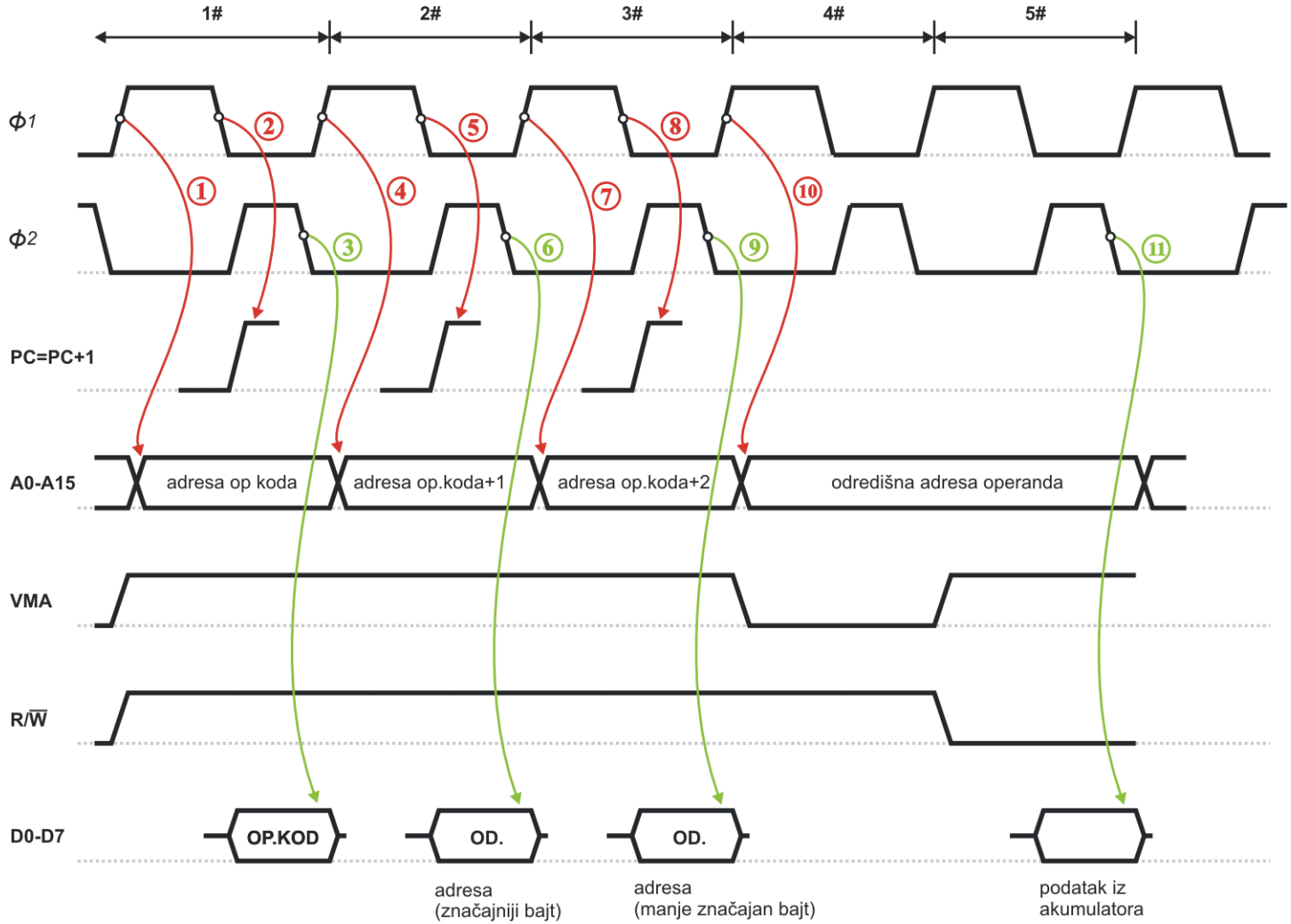
Signali vremenskog vođenja Φ 1 i Φ2



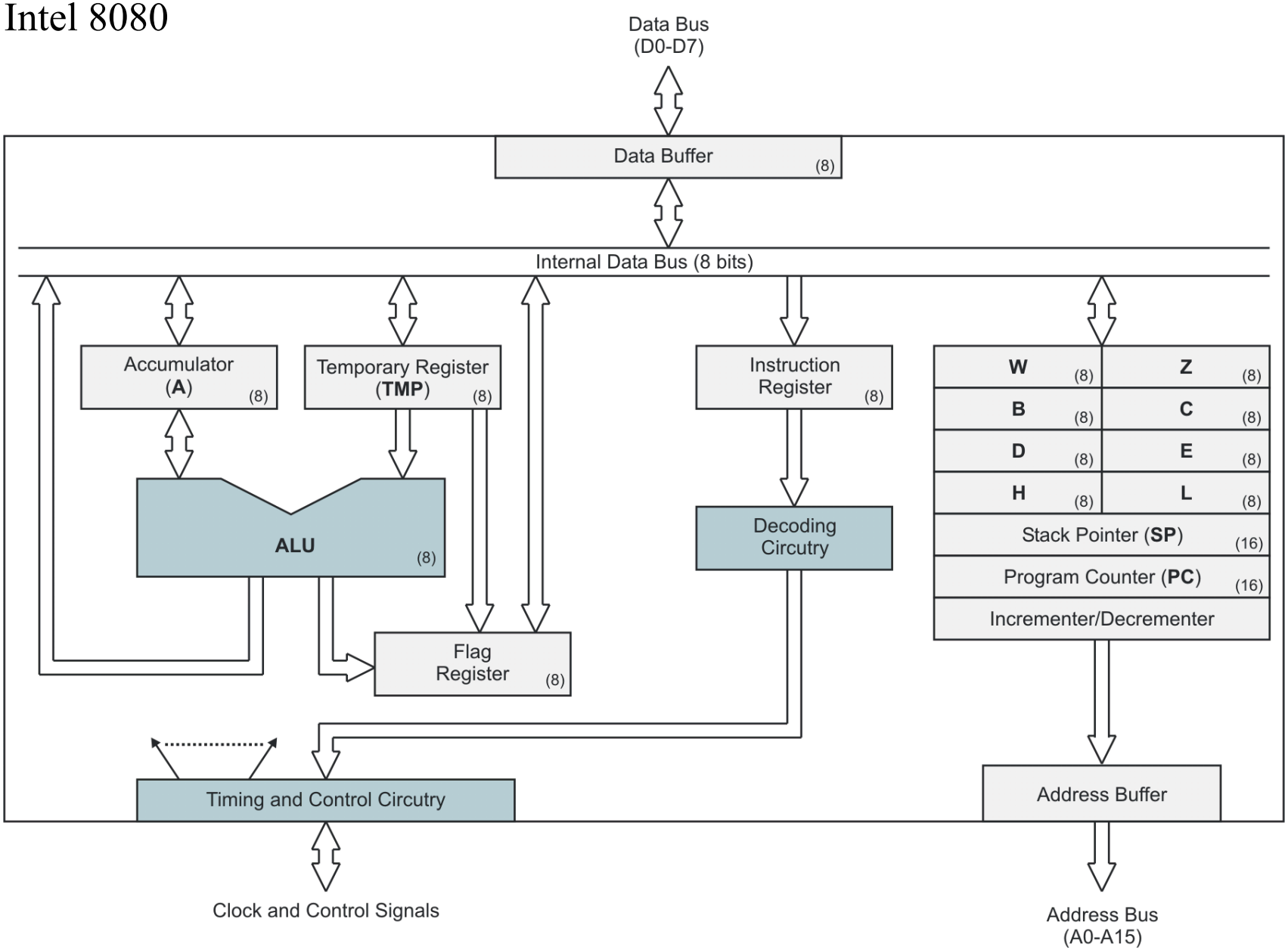
MC 6800


Data Bus
(D0-D7)
Data Buffer
(8)
Internal Data Bus (8 bits)
A Accumulator
(8)
B Accumulator
(8)
Instruction Register
(8)
X
Index Register
(16)
PC
Program Counter
(16)
S
Stack Pointer
(16)
ALU
Decoding
Circutry
Z
N
Flags (CCR)
8
8
Timing and Control Circutry
Address Buffer
(16)
Clock and Control Signals
Address Bus
(A0-A15)

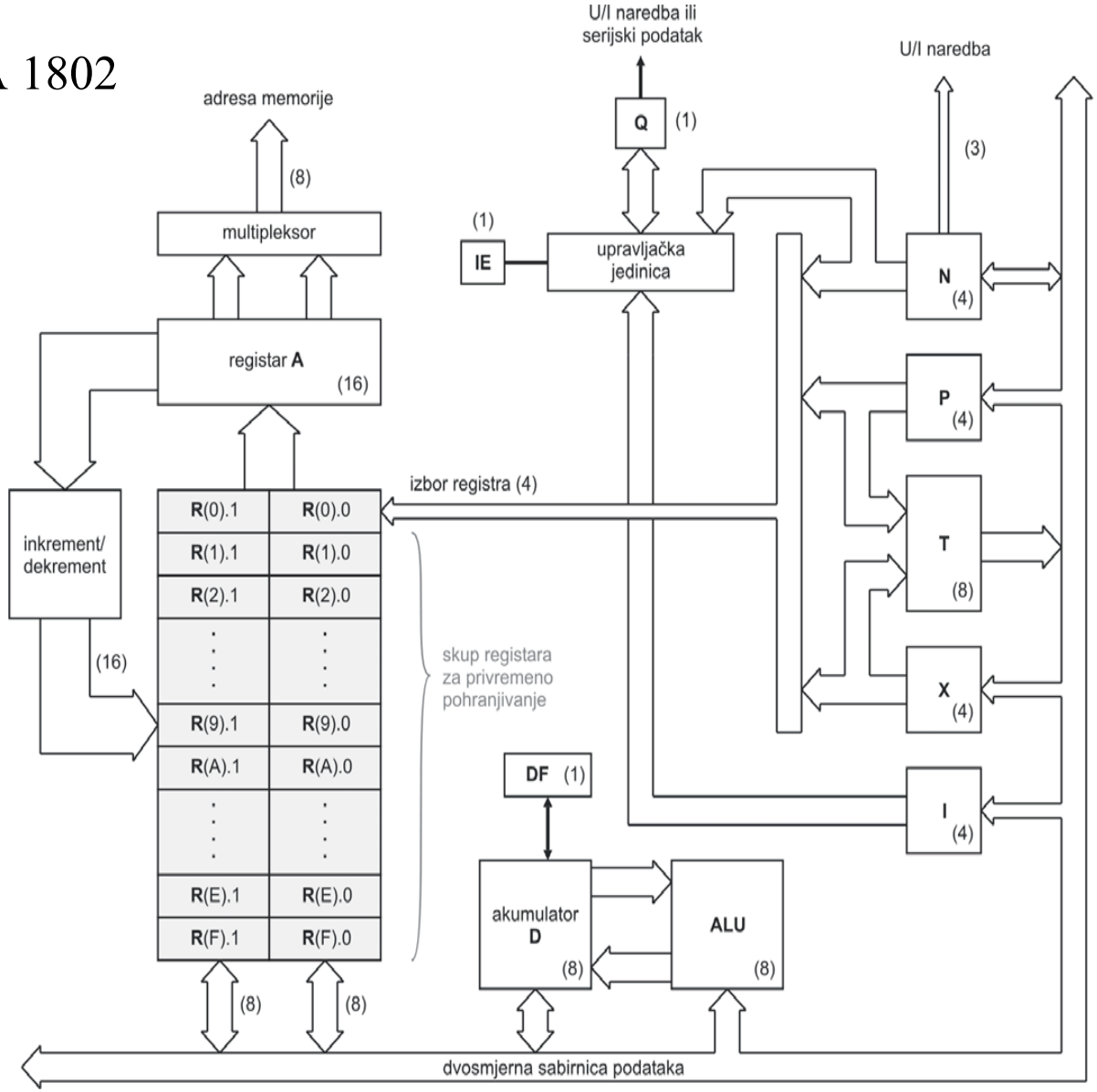
Stanje na sabirnicama za STA A $010F (MC 6800)

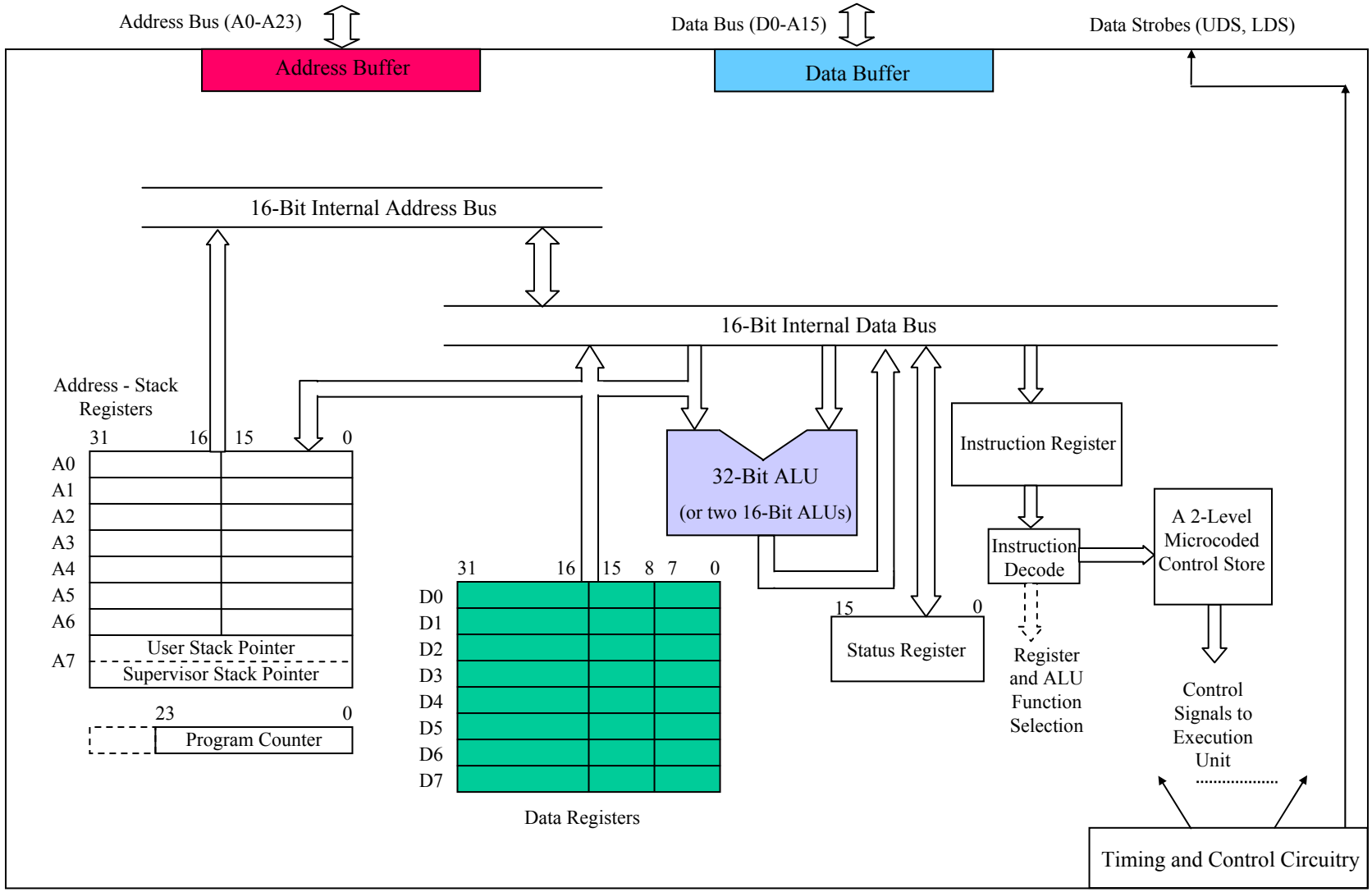


Intel 8080

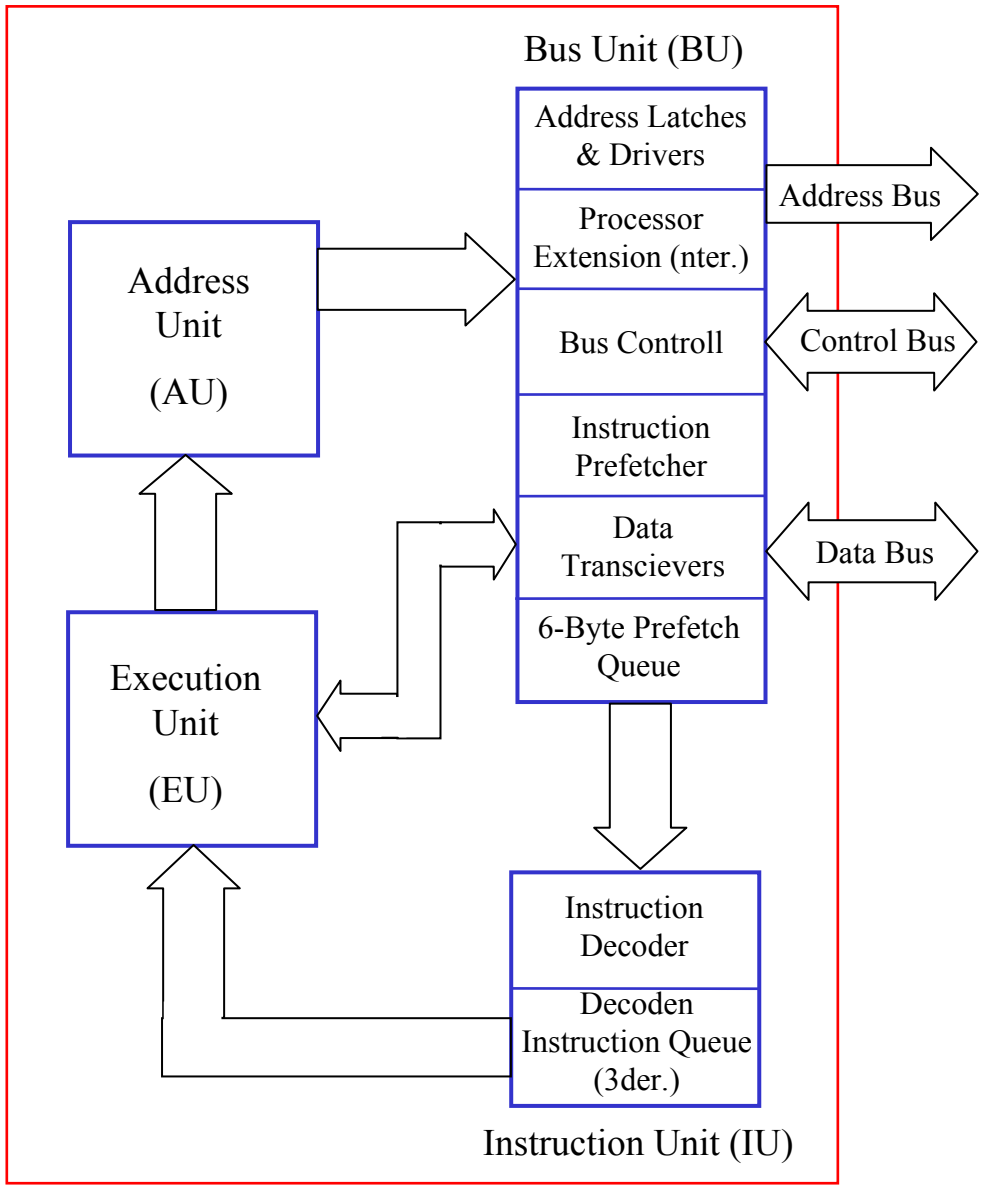

Data Bus
(D0-D7)
Data Buffer
(8)
Internal Data Bus (8 bits)
Accumulator
(A)
(8)
Temporary Register
(TMP)
(8)
Instruction
Register
(8)
W
(8)
Z
(8)
B
(8)
C
(8)
D
(8)
E
(8)
H
(8)
L
(8)
ALU
(8)
Decoding
Circuitry
Stack Pointer (SP)
(16)
Program Counter (PC)
(16)
Incrementer/Decrementer
Flag
Register
(8)
Timing and Control Circuitry
Address Buffer
Clock and Control Signals
Address Bus
(A0-A15)

RCA 1802


U/I naredba ili serijski podatak
U/I naredba
adresa memorije
Q
(1)
(3)
(8)
multipleksor
(1)
IE
upravljačka jedinica
N
(4)
registar A
(16)
P
(4)
izbor registra (4)
inkrement/ dekrement
R(0).1
R(0).0
R(1).1
R(1).0
R(2).1
R(2).0
T
(8)
(16)
skup registara za privremeno pohranjivanje
X
(4)
R(9).1
R(9).0
R(A).1
R(A).0
DF (1)
I
(4)
akumulator D
(8)
ALU
(8)
R(E).1
R(E).0
R(F).1
R(F).0
(8)
(8)
dvosmjerna sabirnica podataka


Address Bus (A0-A23)
Data Bus (D0-A15)
Data Strobes (UDS, LDS)
Address Buffer
Data Buffer
16-Bit Internal Address Bus
16-Bit Internal Data Bus
Address - Stack Registers
31
16
15
0
A0
A1
A2
A3
A4
A5
A6
A7
User Stack Pointer
Supervisor Stack Pointer
23
0
Program Counter
32-Bit ALU
(or two 16-Bit ALUs)
31
16
15
8
7
0
D0
D1
D2
D3
D4
D5
D6
D7
Data Registers
15
0
Status Register
Instruction Register
Instruction Decode
A 2-Level Microcoded Control Store
Register and ALU Function Selection
Control Signals to Execution Unit
Timing and Control Circuitry

Intel 80286


Bus Unit (BU)
Address Latches & Drivers
Processor Extension (nter.)
Bus Controll
Instruction Prefetcher
Data Transcievers
6-Byte Prefetch Queue
Address Bus
Control Bus
Data Bus
Address Unit (AU)
Execution Unit (EU)
Instruction Decoder
Decoden Instruction Queue (3der.)
Instruction Unit (IU)

Intel 80286 i 80386

• CLOCK input

Frekvencija signala na ulazu CLOCK interno se dijeli s 2:

fPCLOCK(ProcessorCLOCK) = ½ fCLOCK

Intel 486 DX

fPCLOCK(ProcessorCLOCK) = fCLOCK

Proizvođači se obično referenciraju na PCLOCK

Intel 486 DX4

fPCLOCK(ProcessorCLOCK) = 2fCLOCK
3fCLOCK

Izvor: T. Shanley, D. Anderson, ISA System Architecture, Addison-Wesley, 1995.

Sabirnički ciklus

Kada procesor izvodi operaciju ČITANJA ili PISANJA, započinje sljed događaja koji se naziva SABIRNIČKI CIKLUS (Bus Cycle).

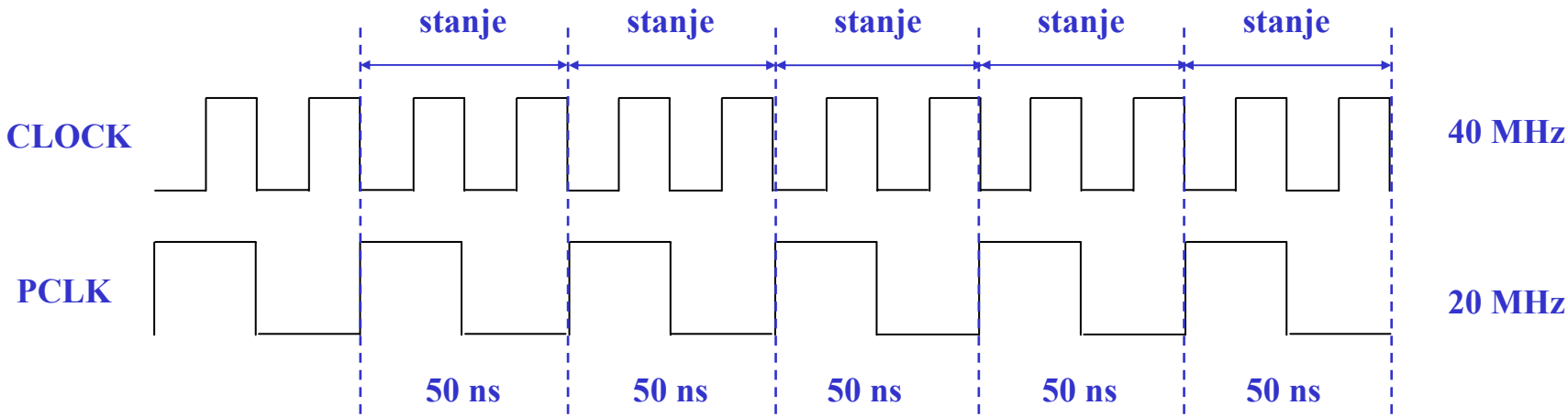
Tijekom sabirničkog ciklusa:

- procesor postavlja adresu na adresnu sabirnicu
- generira upravljačke signale i postavlja ih na upravljačku sabirnicu
- označava vrstu prijenosa
- prenose se podaci između ciljne lokacije i procesora

x86 procesori imaju podsustav – sabirničku jedinicu (bus unit) koja podržava sabirnički ciklus

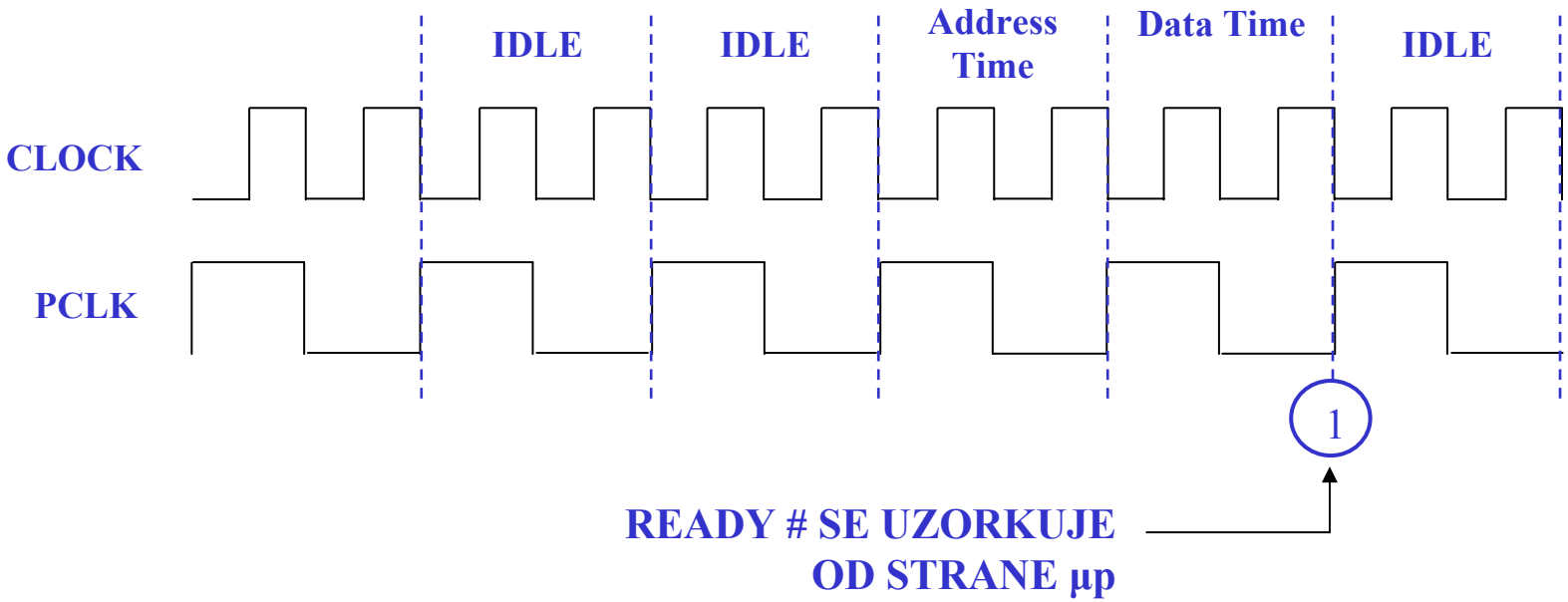
Sabirnička jedinica – stroj stanja

Vrijeme trajanja stanja ⟶ perioda PCLOCK-a



Stanja:

- Vrijeme neaktivnosti (Idle)
- Vrijeme adresiranja (Address Time)
- Vrijeme podataka (Data Time)



Vrijeme adresiranja:

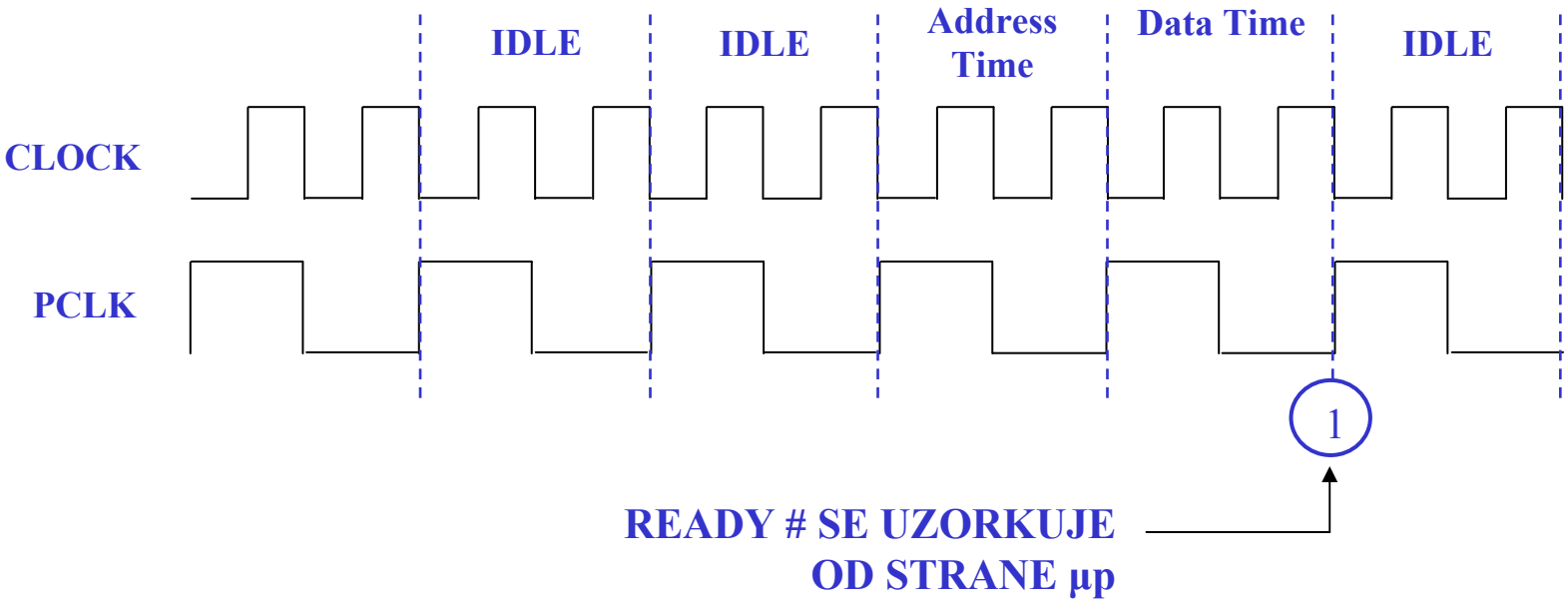
-sabirnička jedinica započinje sabirnički ciklus
iz stanja IDLE prelazi u stanje Vrijeme adresiranja
-Tijekom tog stanja (traje jednu periodu PCLOCK-a) sabirnička jedinica postavlja adresu na adresnu sabirnicu a na upravljačku sabirnicu postavlja informaciju o vrsti sabirničkog ciklusa

Vrijeme podataka:

- Iz stanja Vremena adresiranja sabirnička jedinica prelazi u stanje Vrijeme podataka

-Tijekom tog stanja (traje jednu periodu PCLOCK-a) sabirnička jedinica obavlja prijenos podataka
- Na kraju tog stanja, sinkrono sa signalom PCLOCK, procesor ispituje stanje READY# ulaza
- Ako je READY# nisko, tj. logičko "0" sabirnička jedinica završava sabirnički ciklus

0 – Wait-state bus cycle (sabirnički ciklus sa nula stanja čekanja)



Najbrži sabirnički ciklus x86 procesora traje dvije periode PCLOCK-a

ISA sabirnica (Industry Standard Architecture)

- Proširenje IBM PC sabirnice /temelji se Intel 8088 sustavima
- 62 signalne linije (20 linija za adresiranje, 8 linija podataka, te upravljačke linije (npr., Memory read, Memory Write, I/O read, I/O write, linije za zahtijevanje prekida, potvrdu prekida, te linije za DMA)
- Frekvencija (PCLOCK-a) 8.33MHz /brzina prijenosa 4.166MB/s ili 8.33 MB/s (za 16 bitnu sabirnicu podataka)

EISA (Extended ISA)

- 32-bitna adresna sabirnica
- 8-, 16- ili 32-bitni prijenos podataka
- Brzina prijenosa 33 MB/s

PCI (Peripheral Component Interconnect Bus)

Potreba za većom propusnosti sabirnice!

Primjer:

Slika /zaslon/ rezolucije 1024 x 768 slikovnih elemenata (pixel) –true color (3 bajta/pixel)

1 zaslon = 2.25 MB podataka

Slika u pokretu: 30 zaslona/s.

Potrebna brzina: 67.5 MB/s

Prikaz video zapisa sa čvrstog diska, CD-ROM-a ili DVD-a
- podaci se s diska preko sabirnice prenose u memoriju i tek tada, da bi se prikazali, putuju preko sabirnice prema grafičkoj kartici

Potrebna brzina prijenosa 135 MB/s!

/to je samo za video – ne uzimajući u obzir potrebe CPU-a i drugih uređaja priključenih na sabirnicu/

Intel, 1990. godine uvodi PCI sabirnicu za računala temeljena na njihovim procesorima
Pentium,
Sun – Ultra SPARC II

Izvorno: PCI prenosi 32 bita/perioda i radi na 33 MHz (perioda 30 ns)

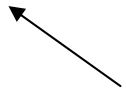
- Brzina prijenosa 133 MB/s

1993. godine: PCI 2.0
1995. godine: PCI 2.1

PCI 2.2

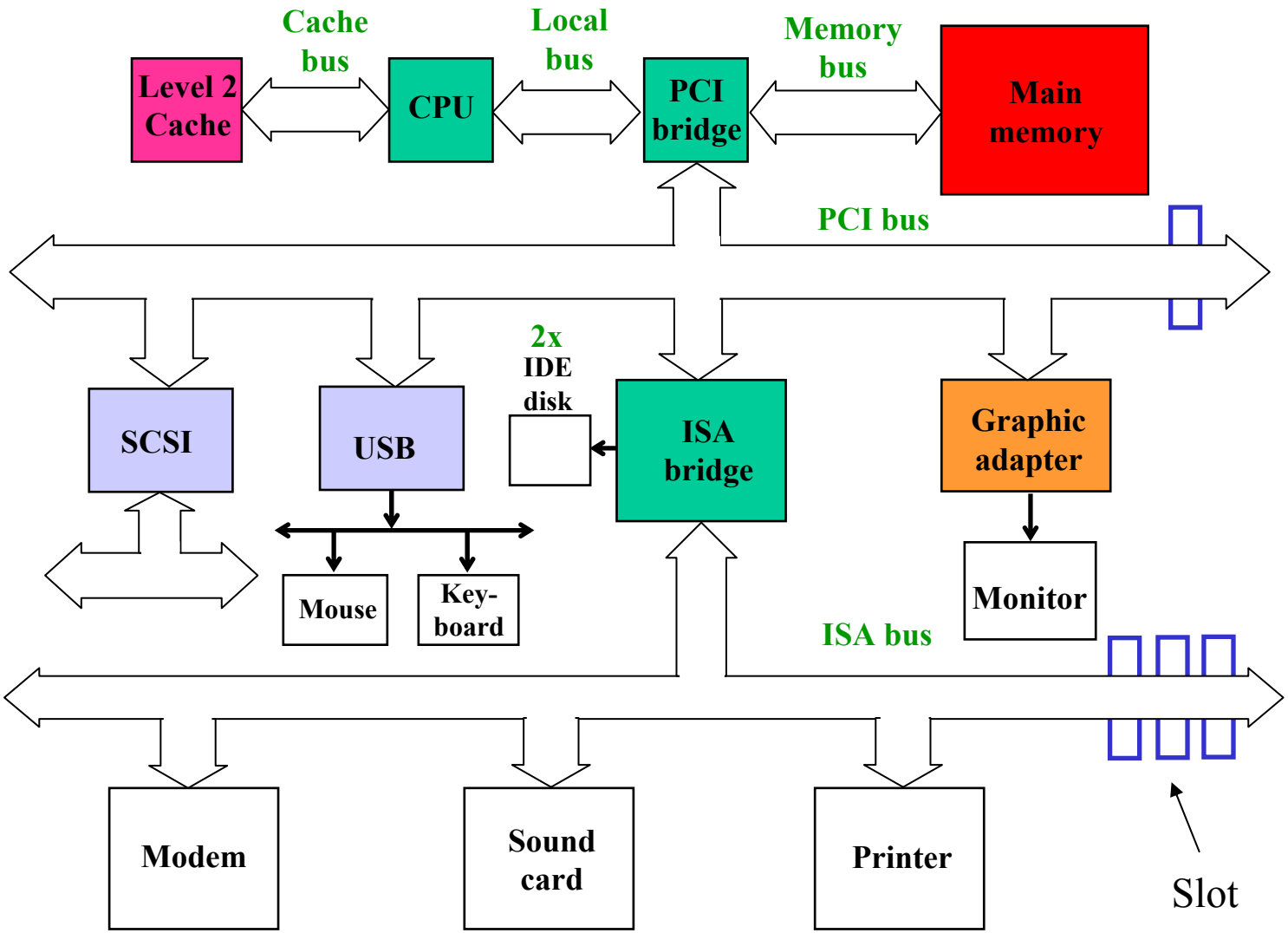
-66 MHz i rukuje 64-bitnim prijenosom

- Brzina prijenosa 528 MB/s



Još uvijek nije dovoljna brzina prijenosa (npr., za memorijsku sabirnicu)
Brzina nije kompatibilna s ISA/EISA modulima

Intel ponudio rješenje:



IDE - Integrated Drive Electronics

EIDE – Extended IDE (adresna shema LBA /Logical Block Address; 0 do $2^{24} - 1$ broj sektora; kapacitet diskova ≥ 528 MB/)

USB - Universal Serial Bus

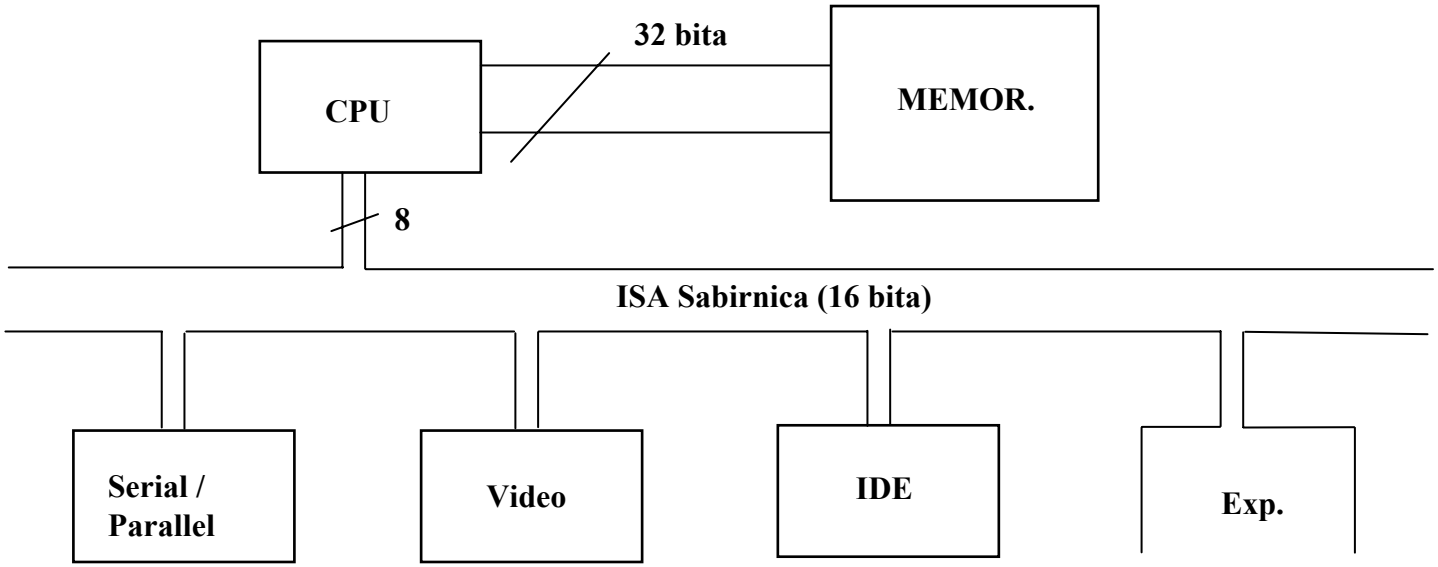
- USB male brzine: 1.5 Mbita/s (USB 1.0)
- USB srednje brzine: 12 Mbita/s (USB 1.0)
- USB velike brzine: 480 Mbita/s (USB 2.0)

SCSI - Small Computer System Interface

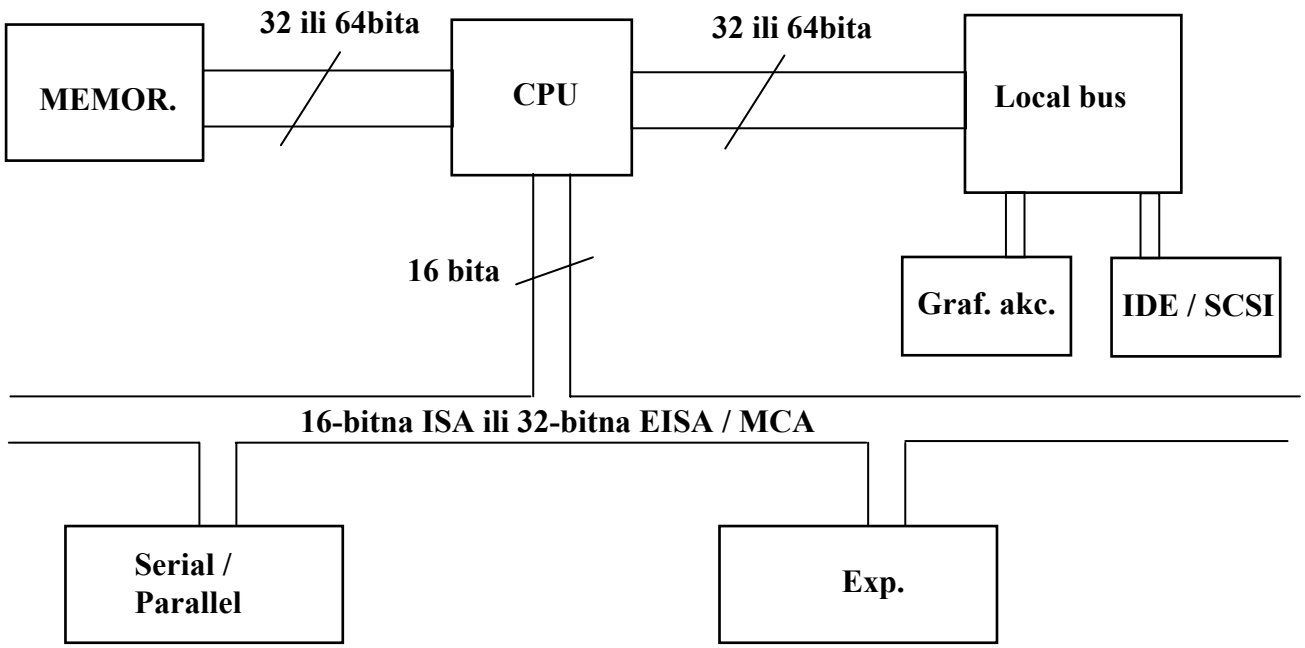
Neke značajke SCSI

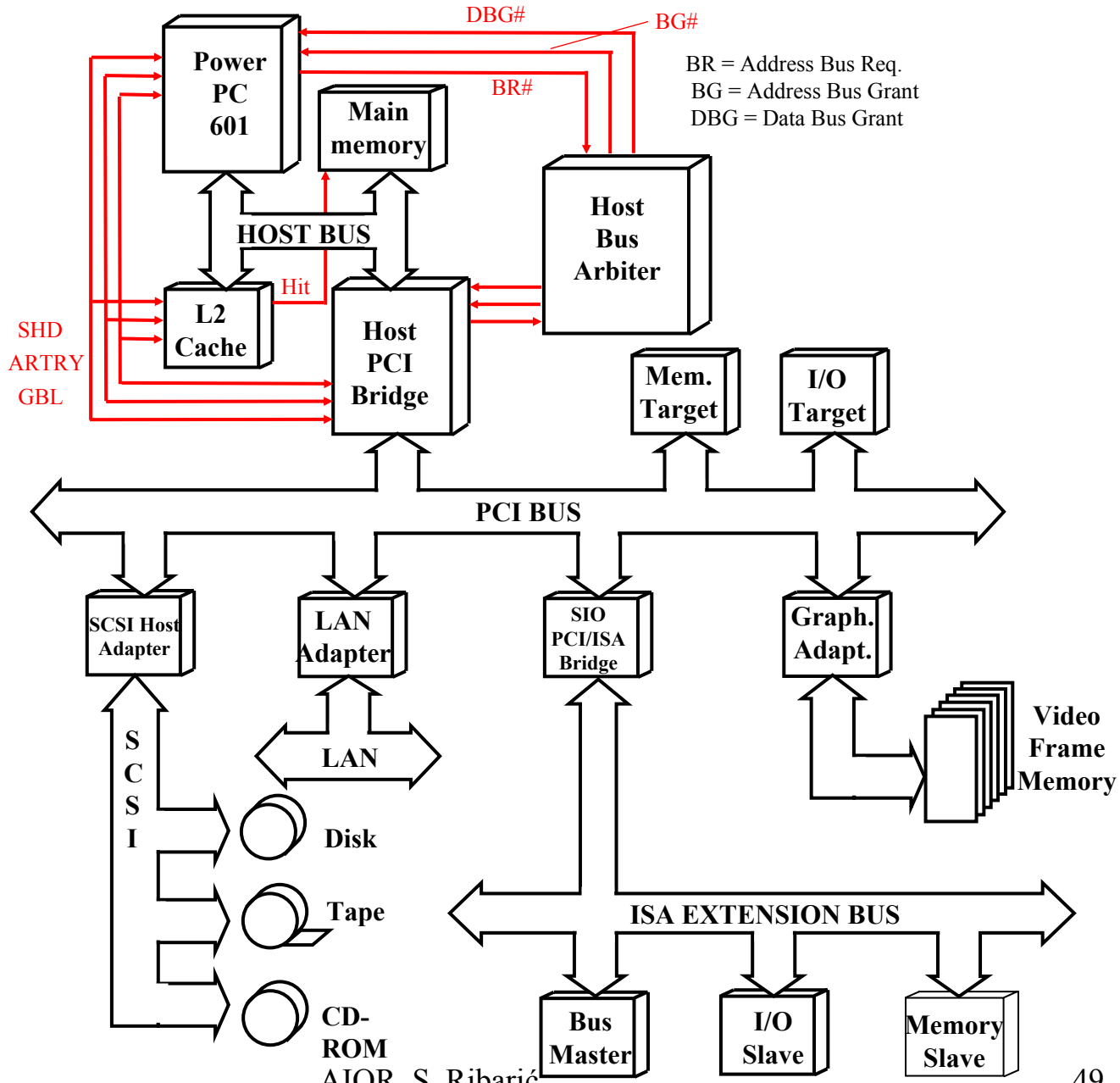
Naziv	Broj bitova	Frekvencija sabirnice(MHz)	MB/s
SCSI-1	8	5	5
Fast SCSI	8	10	10
Wide Fast SCSI	16	10	20
Ultra SCSI	8	20	20
Wide Ultra SCSI	16	20	40
Ultra2 SCSI	8	40	40
Wide Ultra2 SCSI	16	40	80

PC - 1986. godina



PC – 1993. godine

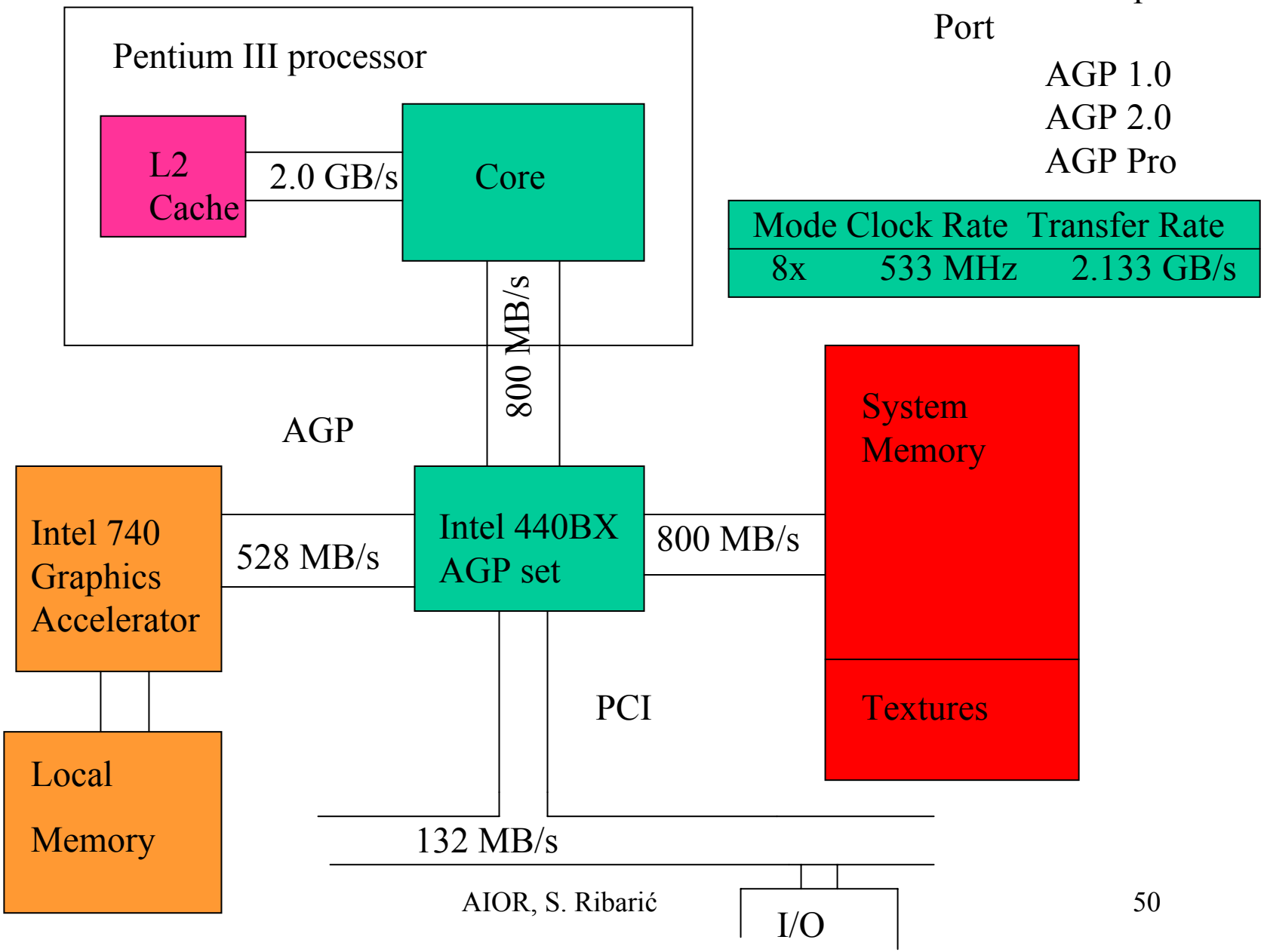



DBG#
BG#
BR#
BR = Address Bus Req.
BG = Address Bus Grant
DBG = Data Bus Grant
Power PC 601
Main memory
HOST BUS
Host Bus Arbiter
Hit
L2 Cache
Host PCI Bridge
SHD
ARTRY
GBL
Mem. Target
I/O Target
PCI BUS
SCSI Host Adapter
LAN Adapter
SIO PCI/ISA Bridge
Graph. Adapt.
Video Frame Memory
LAN
SCSI
Disk
Tape
CD-ROM
ISA EXTENSION BUS
Bus Master
I/O Slave
Memory Slave

AGP – Accelerated Graphic Port

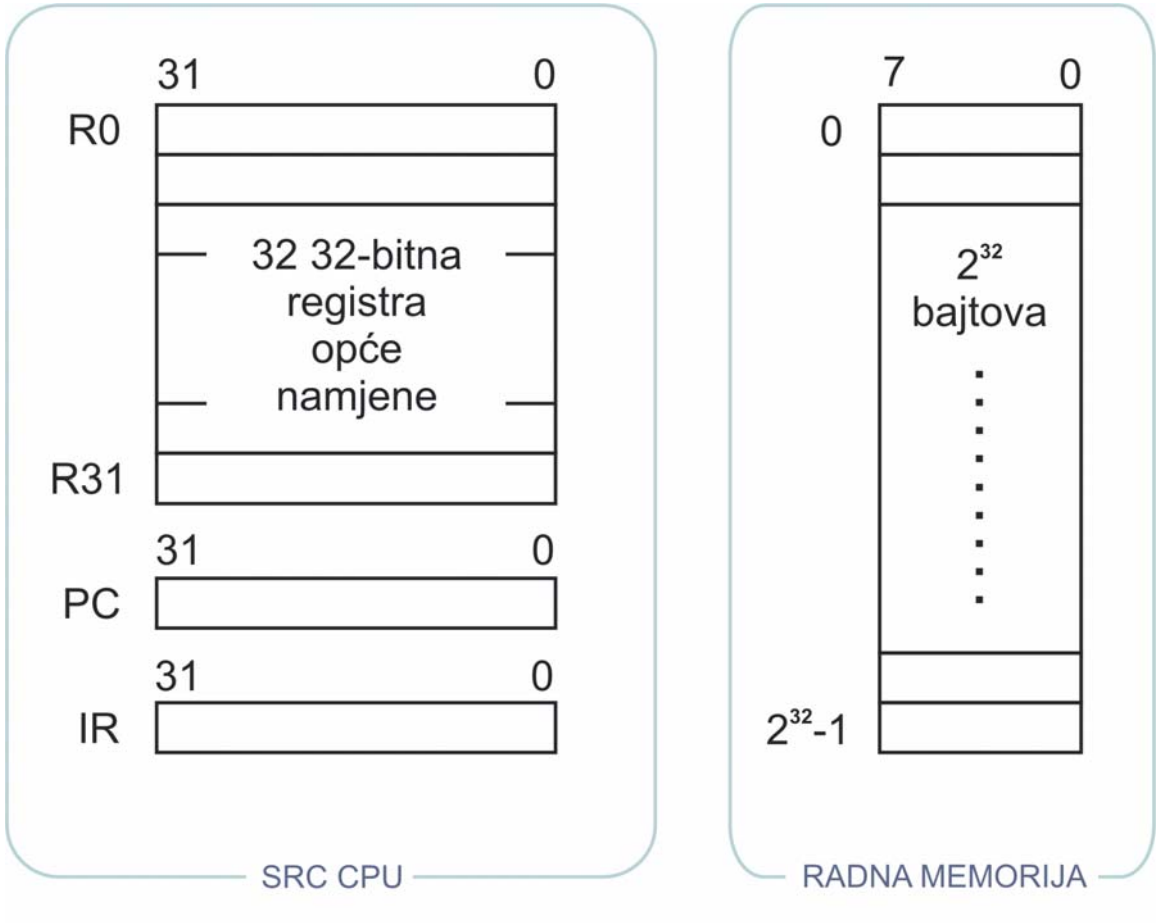
AGP 1.0
AGP 2.0
AGP Pro

Mode	Clock Rate	Transfer Rate
8x	533 MHz	2.133 GB/s



SRISC – Simple RISC

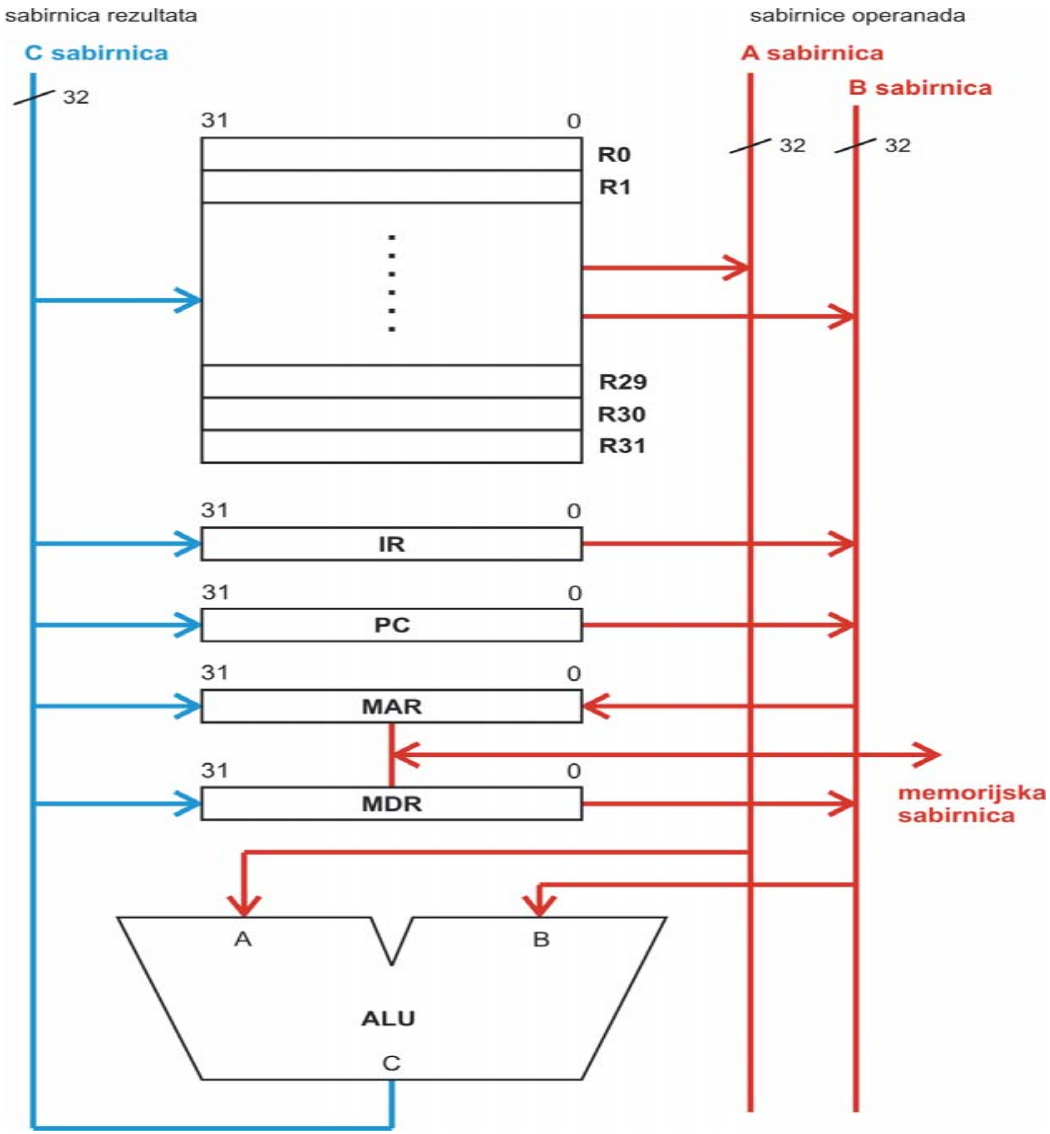
- Programski model



Značajke:

- Memorija bajtno organizirana – dohvat samo 32-bitne riječi
- *load/store* arhitektura
- Big – Endian Byte Ordering

Trosabirnički SRISC

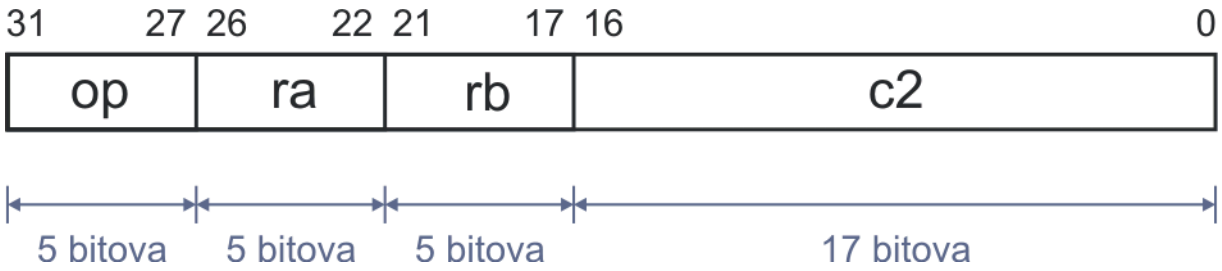


ISA – Instruction Set Architecture

SRISC ima osam različitih formata instrukcija:

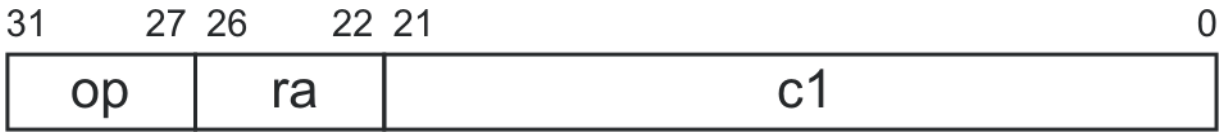
1. format

Instrukcije: *ld, st, la, addi, andi, ori*



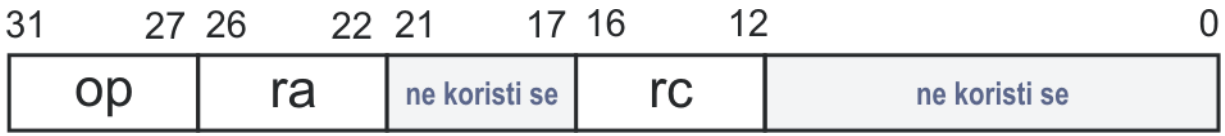
2. format

Instrukcije: *ldr, str, lar*



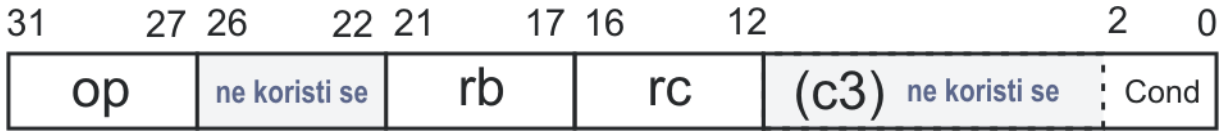
3. format

Instrukcije: *neg, not*



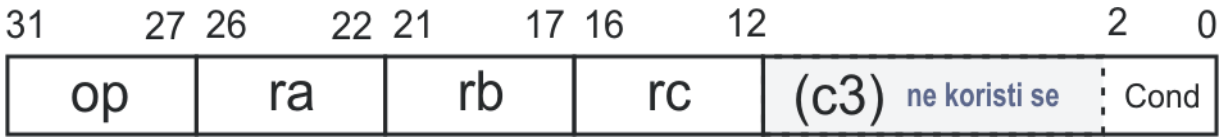
4. format

Instrukcija: *br*



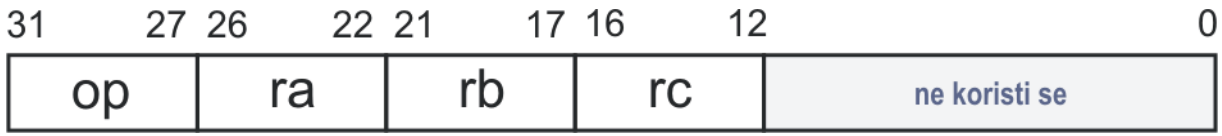
5. format

Instrukcija: *brl*



6. format

Instrukcije: *add, sub, and, or*



Troadresni format instrukcije!

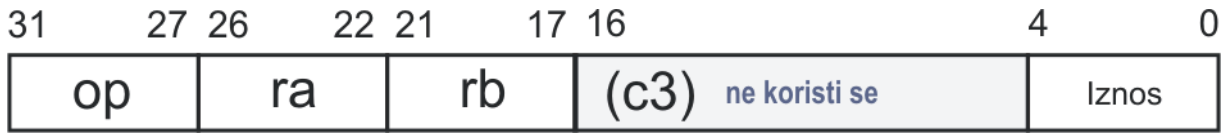
7. format

Instrukcije: *nop, stop*

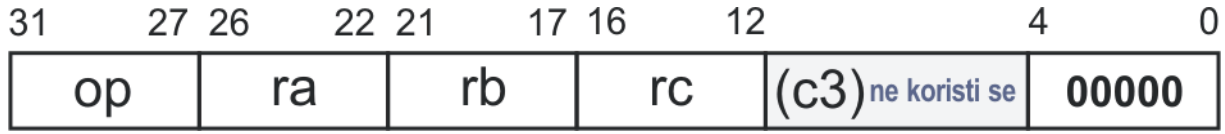
8. format

Instrukcije: *shr, shl*

a)



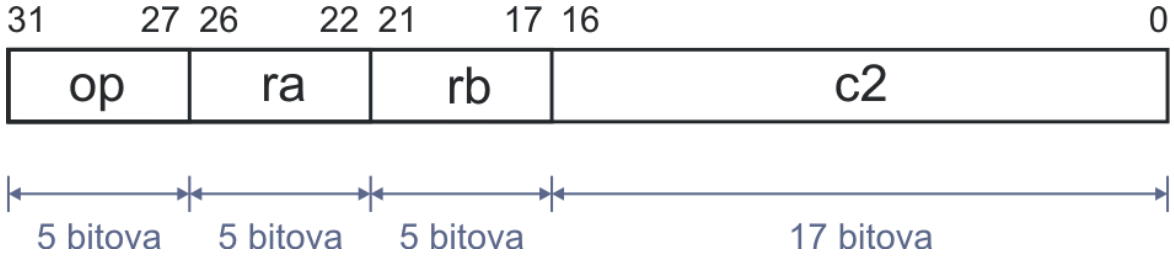
b)



Instrukcije za pristup memoriji (load i store tip instrukcija)

- *load* i *store* **jedine** su instrukcije za dohvat i pohranu operanada iz/u memorije (i):

4 *load* instrukcije: *ld, ldr, la, lar*
2 *store* instrukcije: *st, str*

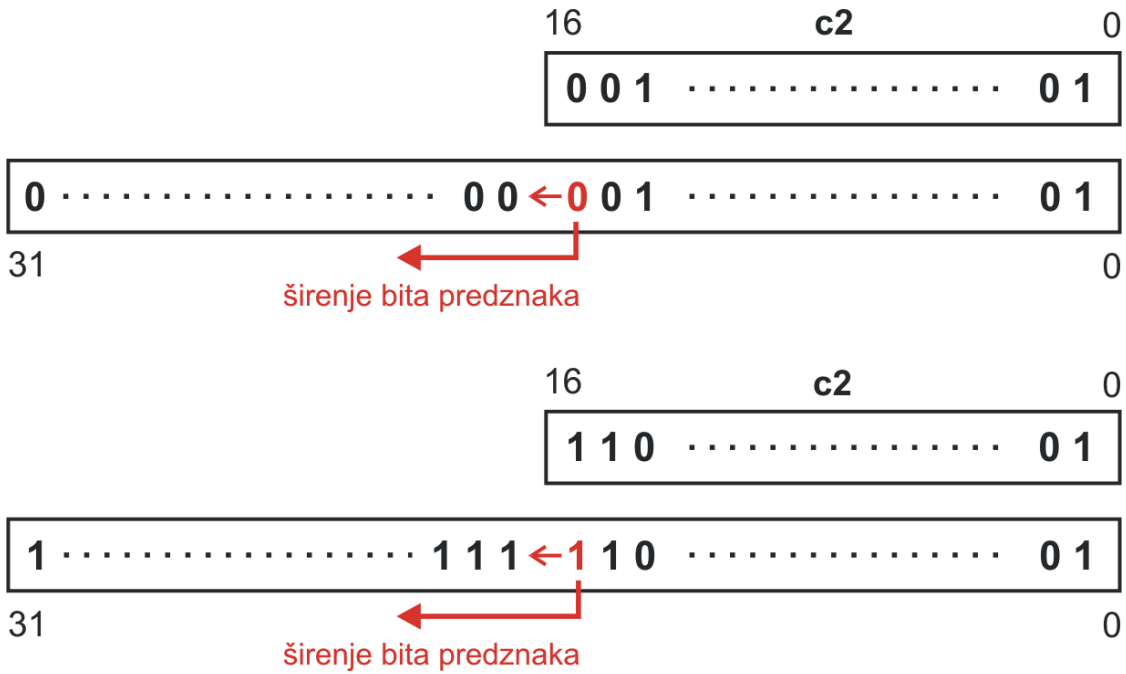


load: /mnemonik ld/

- puni registar određen 5-bitnim poljem *ra* (1. format instrukcije)
- adresa izvorišta određena je 17-bitnom vrijednosti u polju *c2*
- polje *rb* ima dvostruku ulogu:

  1. Ako je *rb* = 0 (00000_B) tada (*rb* = 0) služi kao "signal" upravljačkoj jedinci da je adresa memorijske lokacije (izvorišta) vrijednost *c2* koja se pretvara u 32-bitnu i to **širenjem bita predznaka (engl. sign-extended)**

Širenje bita predznaka



2. Ako je $rb \neq 0$ tada se adresa memorije oblikuje kao $c2$ + R[rb] (based, displacement addressing mode)

POZOR: zbrajanje $c2$ + R[rb] obavlja se TIJEKOM izvođenja instrukcije (engl. run time)

Instrukcije koje koriste 1. format instrukcije:

ld ra, c2 ; izravno (direktno) adresiranje: R[*ra*] = M[*c2*]

ld ra, c2(rb) ; indeksno adresiranje (*rb* $\neq 0$): R[*ra*] = M[*c2* + R[*rb*]]

store: /mnemonik st/

-Instrukcija *st* obavlja "obrnutu" (u odnosu na *ld*) operaciju:

1. Ako *rb* = 0 (00000_B) tada se R[*ra*] pohranjuje na memorijskoj lokaciji s adresom *c2*

2. Ako je *rb* $\neq 0$ tada se R[*ra*] pohranjuje na memorijskoj lokaciji s adresom *c2* + R[*rb*]

Instrukcije koje koriste 1. format instrukcije:

st ra, c2 ; izravno adresiranje M[*c2*] = R[*ra*]

st ra, c2(rb) ; indeksno adresiranje (*rb* $\neq$ 0): M[*c2* + R[*rb*]] = R[*ra*]

Instrukcije koje koriste 1. format instrukcije (nastavak):

la – load address

- računa adresu operanda (kao u prethodnim slučajevima ali umjesto dohvata operanda pohranjuje se izračunata adresa u R[*ra*]

la ra, c2 ; napuni R[*ra*] s adresnim pomaknućem: R[*ra*] = *c2*

la ra, c2(rb) ; napuni R[*ra*] s adresnim pomaknućem: R[*ra*] = *c2* + R[*rb*]

la se koristi za sintezu složenijih načina adresiranja!

Ograničenje izravnog adresiranja

Pazi: *c2* je 17-bitna konstanta

Operandi se nalaze:

1) Na prvih 2^{16} bajtova:

2)

Adresni prostori:

00000000 - 0000FFFF	1. prostor
FFFF0000 – FFFFFFF	2. prostor

Kako ostvariti pristup operandima drugdje u memoriji?

Za pristup operandima drugdje u memorijskom prostoru:

- Adresiranje pomaknućem: R[*rb*] – baza
  c2 – pomaknuće

  efektivna adresa = R[*rb*] + *c2*

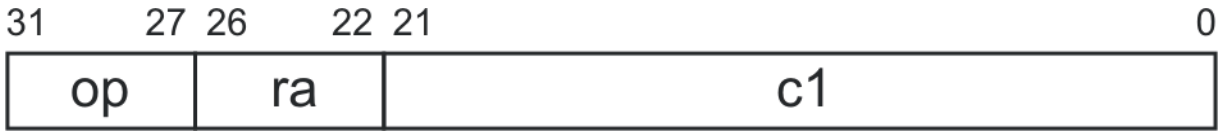
- Indirektno adresiranje: uporaba R[*rb*] pri *c2* = 0

  efektivna adresa = R[*rb*] + 0

POZOR: U postupku računanja (zbrajanja) adrese prvo se 17-bitno pomaknuće treba pretvoriti u 32-bitni broj

Instrukcije: *ldr, str, lar*

Koriste 2. format instrukcije



ldr ra, c1 ; napuni registar R[*ra*] = M [PC + *c1*]
; relativni način adresiranja

str ra, c1 ; pohrani M [PC + *c1*] = R[*ra*]

lar ra, c1 ; napuni relativnu adresu: R[*ra*] = PC + *C1*

POZOR: Efektivna se adresa
oblikuje tijekom izvođenja instrukcije (run-time addition)

Premjestive instrukcije (engl. Relocatable instructions)

- relativne adrese (u odnosu na PC) čine instrukcije premjestivim – cijeli se programski moduli mogu premještati bez mijenjanja vrijednosti pomaknuća

- *c1* je duljine 22 bita – može se specificirati adresa u prostoru od $\pm 2^{21}$ u odnosu na tekuću instrukciju

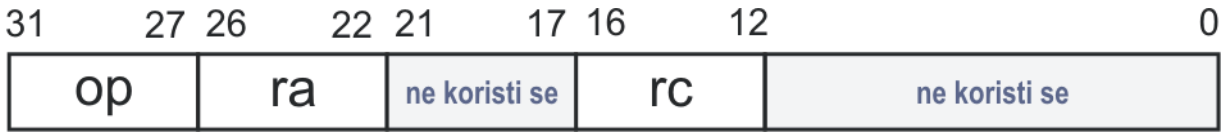
Primjeri instrukcija *load* i *store*

Instrukcija	op	ra	rb	c1	Komentar	Način adresiranja
`ld r1,32`	1	1	0	32	R[1] ← M[32]	Izravno
`ld r22,24(r4)`	1	22	4	24	R[22] ← M[24+R[4]]	Pomaknuće
`st r4,0(r9)`	3	4	9	0	M[R[9]] ← R[4]	Reg.Indirektno
`la r7,32`	5	7	0	32	R[7] ← 32	Usputno
`ldr r12,-48`	2	12	-	-48	R[12] ← M[PC-48]	Relativno
`lar r3,0`	6	3	-	0	R[3] ← PC	Registar

Aritmetičke i logičke instrukcije

• Instrukcije s jednim operandom

- Koriste 3. format instrukcije:

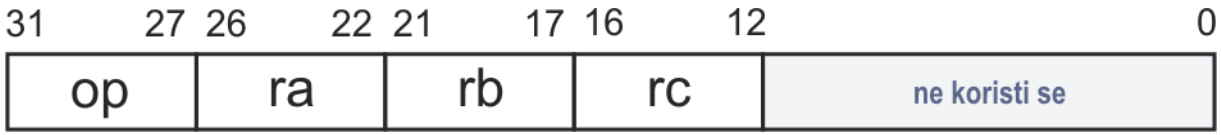


neg ra, rc ; R[*ra*] = - R[*rc*] / dvojni komplement/

not ra, rc ; R[*ra*] = $\overline{\text{R[}rc\text{]}}$ /jedinični komplement/

• ALU instrukcije (binarne operacije)

- koriste 6. format instrukcije (troadresni!):



add ra, rb, rc ; R[*ra*] = R[*rb*] + R[*rc*]

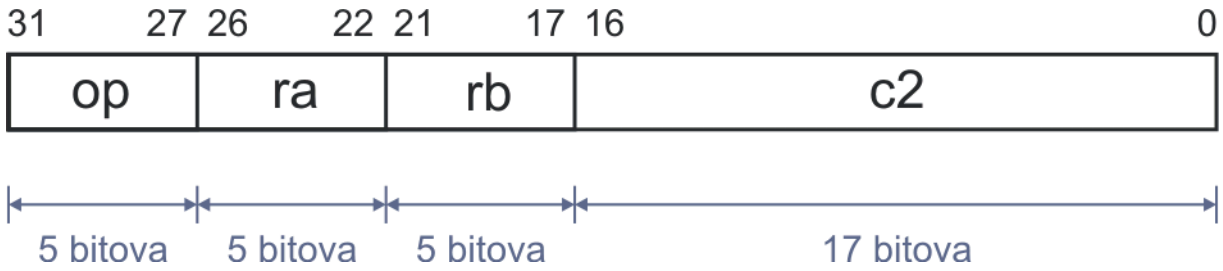
sub ra, rb, rc ; R[*ra*] = R[*rb*] - R[*rc*]

and ra, rb, rc ; R[*ra*] = R[*rb*] $\wedge$ R[*rc*]

or ra, rb, rc ; R[*ra*] = R[*rb*] $\vee$ R[*rc*]

• ALU instrukcije (usputno adresiranje)

- koriste 1. format instrukcije:



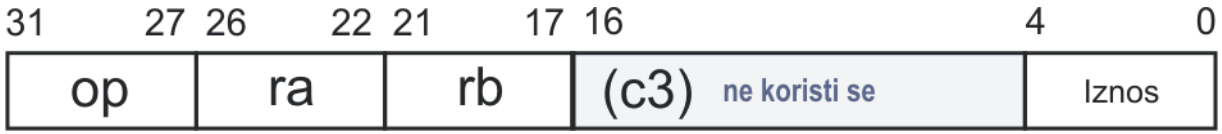
addi ra, rb, c2 ; R[*ra*] = R[*rb*] + *c2* : *c2 – usputna konstanta*

andi ra, rb, c2 ; R[*ra*] = R[*rb*] $\wedge$ *c2*

ori ra, rb, c2 ; R[*ra*] = R[*rb*] $\vee$ *c2*

• Posmačne instrukcije

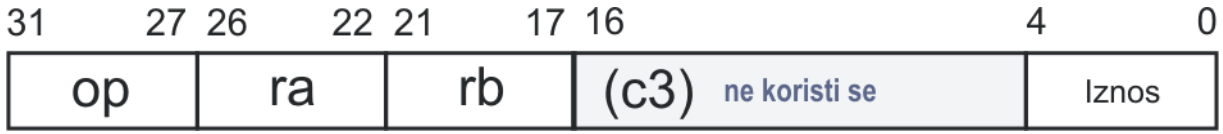
- koriste 8a) format instrukcije:



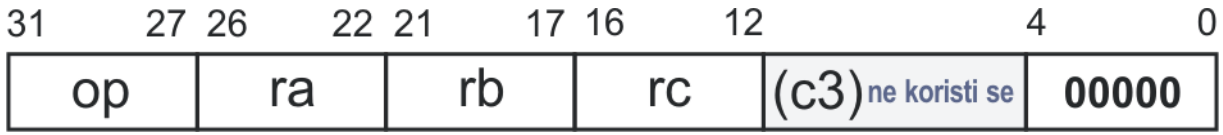
Instrukcije posmiču operand iz R[*rb*] (udesno, ulijevo ili kružno) i smještavaju rezultat u R[*ra*].

Broj posmaknutih mjesta određen je 5-bitnim nepredznačenim brojem

5-bitna vrijednost → iznos posmaka od 0 do 31



Ako je ta vrijednost 0 onda se kao iznos posmaka uzima 5 LSb registra R[*rc*] (format 8b))

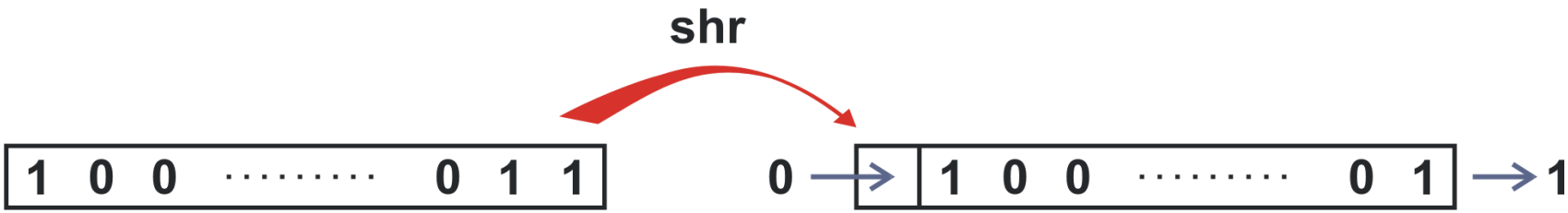


-Razlikujemo dvije vrste posmaka:

1) logički posmak
2) aritmetički posmak

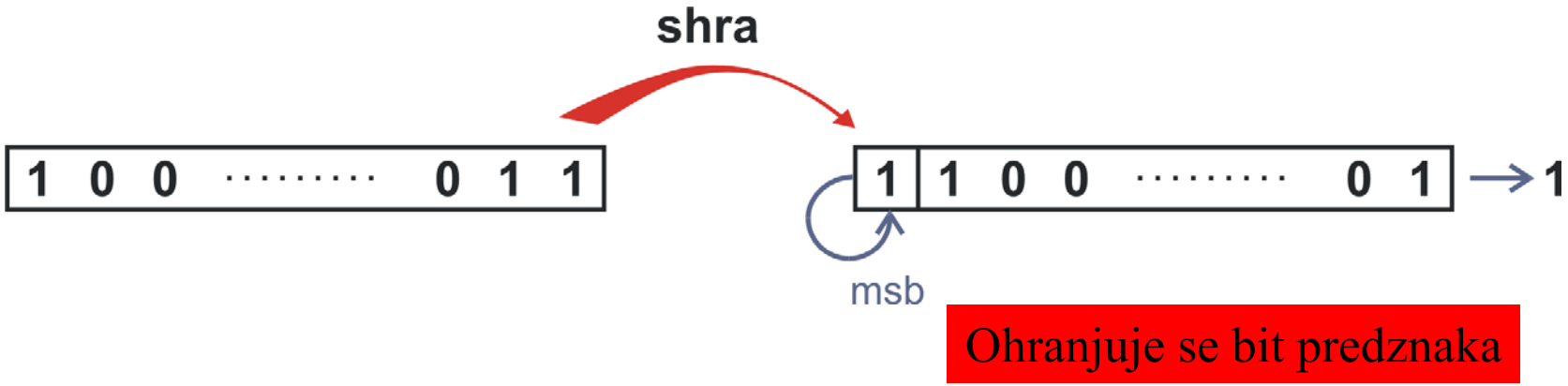
Primjer:

shr logički posmak udesno



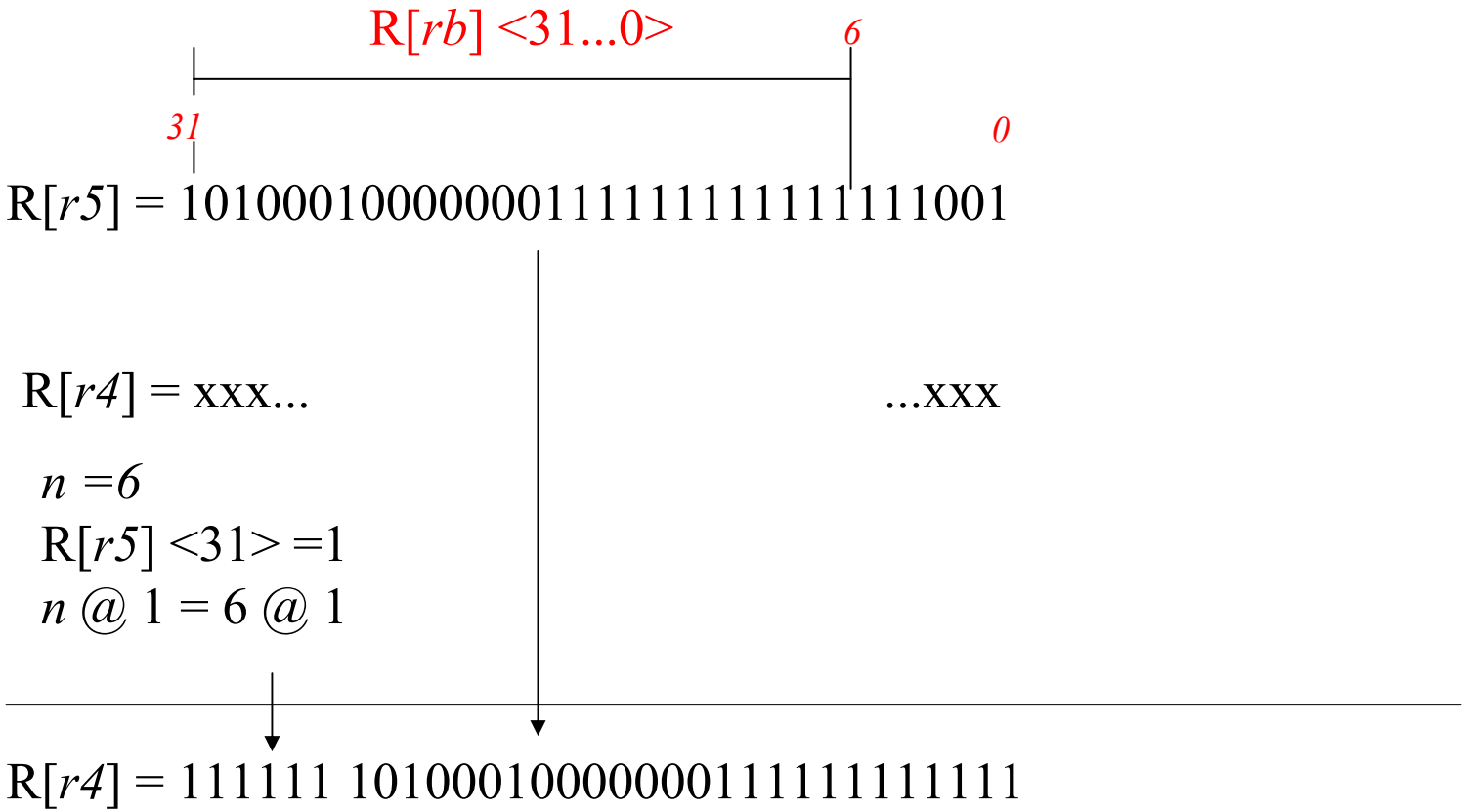
Primjer:

shra aritmetički posmak udesno



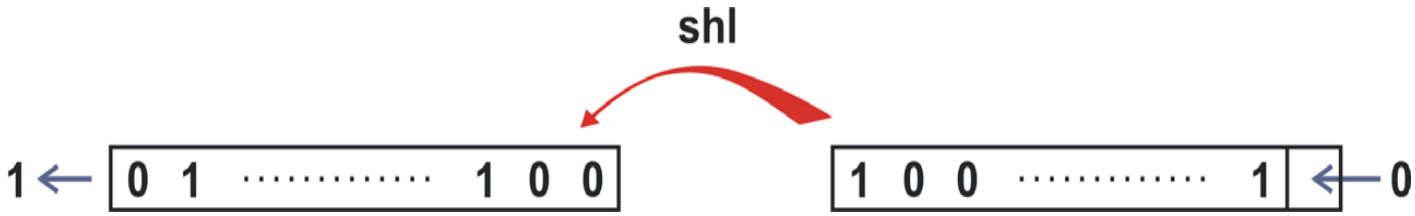
shra (:=op = 27) → R[*ra*] <31...0> ← (*n*@R[*rb*] <31>) # R[*rb*] <31...n>

shra r4, r5, 6



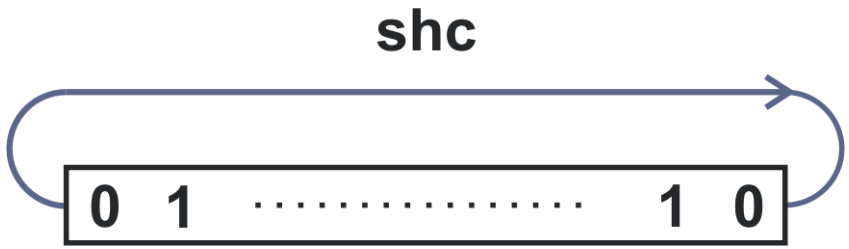
Posmak ulijevo

shl



Kružni posmak

shc



Posmačne instrukcije – primjeri:

shr ra, rb, rc ; posmakni R[*rb*] (za broj mjesta koji je određen s R[*rc*]) i pohrani ga u R[*ra*]

shr ra, rb, count ; posmakni R[*ra*] udesno i pohrani ga u R[*ra*] (za broj mjesta određen u 0-4 polju c3)

shra ra, rb, rc

shl ra, rb, rc

shl ra, rb, count

shc ra, rb, rc

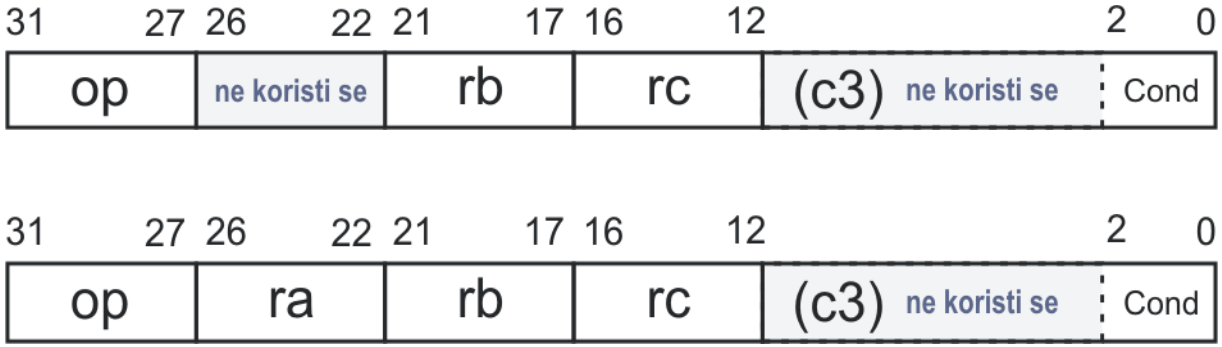
shc ra, rb, count

*A*ko je *count* polje u instrukciji 0 (format 8b) tada se za broj mjesta *posmaka* uzima iz registra koji je određen bitovima instrukcije na poziciji 12 - 16

Instrukcije grananja

br i *brl*

Instrukcije koriste 4. i 5. format:



Instrukcija *br* se izvodi tako da se mijenja sadržaj PC s ciljnom adresom

Instrukcija *brl* (branch&link) se izvodi tako da kopira PC u povezni (engl. linkage) registar i to prije grananja

Povezni registar dopušta povratak iz potprograma i rabi se za implementaciju procedura i funkcija u HLL

Pozor: PC se kopira u povezni registar bez obzira da li će se grananje izvesti (ili ne)

Instrukcije grananja (uvjeti!):

zbirni jezik	*c3*<2...0>	Uvjeti grananja
brnv, brlnv	*0*	*Nikada*
br, brl	*1*	*Bezuvjetno*
brzr, brlzr	*2*	*Ako je* R[*rc*] = 0
brnz, brlnz	*3*	*Ako je* R[*rc*] ≠ 0
brpl, brlpl	*4*	*Ako je* R[*rc*]<31> = 0
brmi, brlmi	*5*	*Ako je* R[*rc*] < 0

Primjer:

brl ra, rc, c3 ; R[*ra*] ← PC i granaj na ciljnu
; adresu određenu s R[*rb*] ako je
; zadovoljen uvjet *c3*

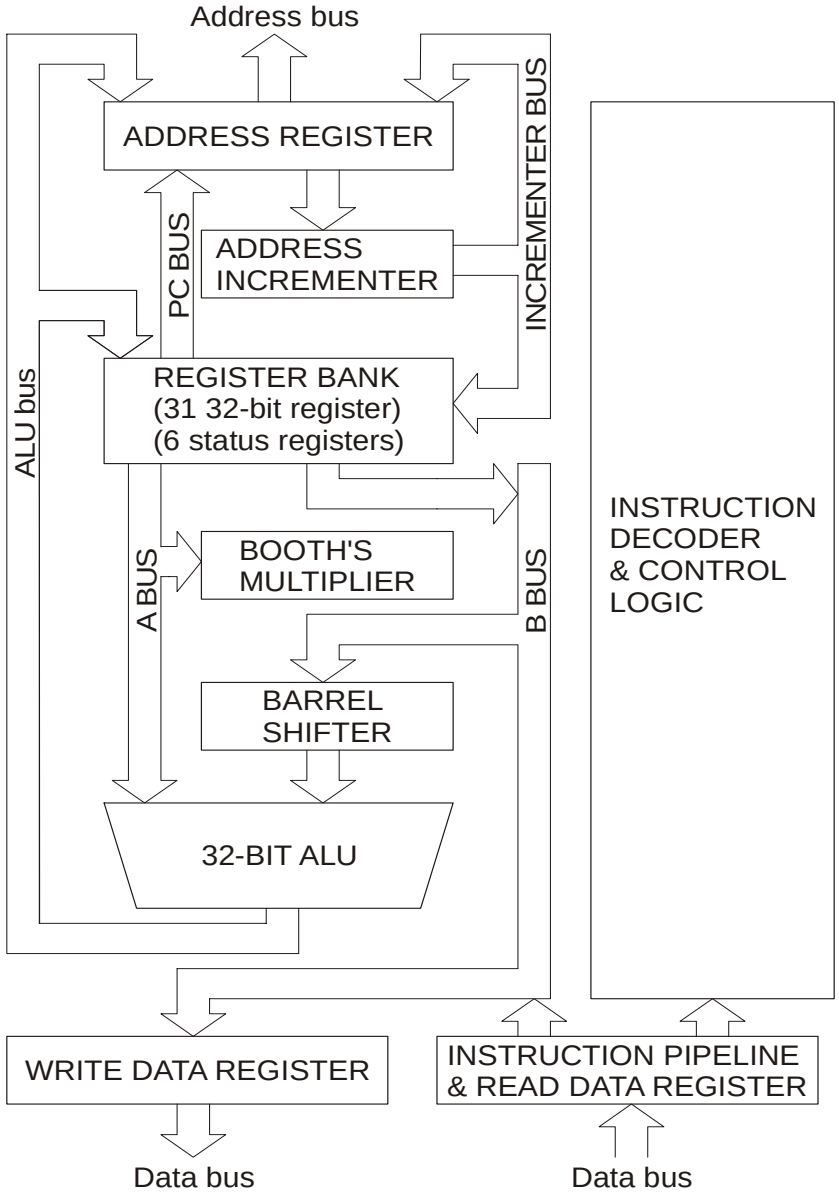
Mješovite instrukcije

nop ; ne čini ništa

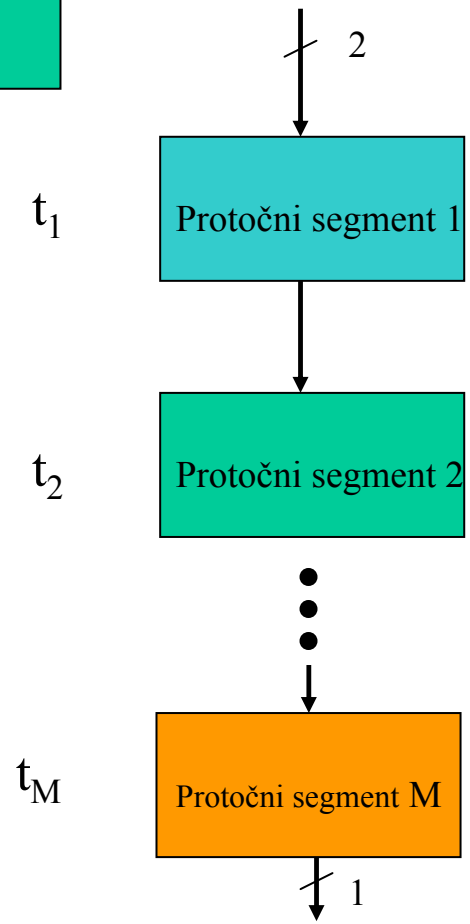
stop ; zaustavi stroj

nop ??? ⟶ *važna instrukcija u protočnoj izvedbi procesora!!!*

ARM 6 procesor - Acorn RISC Machine



Model protočne strukture dubine M



- N >> M parova operanada
- Vrijeme obrade u protočnom segmentu: $t_1 = t_2 = ... = t_M = t_S$

Prvi rezultat: $M \cdot t_S$

Svaki slijedeći rezultat nakon t_s

Vrijeme obrade N parova operanada:

$T_N = Mt_S + (N - 1)\, t_S$

Vrijeme obrade jednog para operanada:

$T_{ef} = T_N / N$

$T_{ef} = (Mt_S + (N - 1)\, t_S) / N$

Vrijeme obrade para operanda:

$$T_{ef} = (Mt_S + (N - 1)\, t_S) / N$$

$$N >> M;\ \ N \rightarrow \infty$$

$$T_{\infty} = \lim_{N \rightarrow \infty} ((Mt_S + (N - 1)\, t_S) / N)$$

Vrijeme obrade jednog para operanada:

$$T_{\infty} = t_S$$!!!

Protočnost – značajka RISC i CISC procesora!